

SSEP/SSE

Synchronous serial ECL interface with programmable oscillators



Description

The SSE is a mezzanine board that pairs with an EDT main board (for PCI or PCI Express) for high-speed data transfer. It supports thirty-two ECL, LVDS, or RS422 signals in groups of four.

The SSE samples the data on the rising edge of the clock and stores it in host memory via the main board. One 15-pin D connector is provided. Each channel accepts a differential data signal (two wires) and a differential clock (two more wires) at standard ECL signal levels. The output channel has one differential data signal and one differential clock. All input signals are terminated through 50 Ω to -2 volts.

The SSE has another differential data signal that can be used in applications where notification of a start or an end of a block transfer is necessary.

The main board supplies high-speed DMA, plus additional memory and programmable FPGA resources.

Features

Mezzanine board – pairs with an EDT main board (in a PCI, PCI-X, or PCIe slot), which adds high-speed DMA, programmable FPGA resources, and memory

Channels 0, 1, 2: Two input and one I/O – one data bit per channel

I/O: Thirty-two ECL, LVDS, or RS422 signals

Data rates up to 400 Mb/s per channel

ECL-compatible drivers/receivers

Reed-Solomon error coding

Two user-defined LEDs

Applications

Telemetry receiver and transmitter

Communications monitoring
(serial data)

Satellite ground station support

Specifications

Product Type	SSEP is a mezzanine board for synchronous serial ECL with programmable oscillators; it requires a main board.	
FPGAs and Memory	Programmable FPGA and memory resources are provided by the main board.	
Clocks	Two clocks (default option) or one clock (legacy option) are available, as described below.	
	Default option (SSEP)	Two (one PLL-based clock synthesizer, programmable from 50 MHz to 800 MHz plus one output VCXO, programmable to any frequency from 10 MHz to 810 MHz)
	Legacy option (SSE)	One PLL-based clock synthesizer, programmable from 50 MHz to 800 MHz
Data Rates	Data rates are dependent on data format and main board.	
Data Format (I/O)	32 ECL, LVDS, or RS422 signals in groups of four	
Reed-Solomon Decoder	Frame synchronizer Frames – check and flywheel Error correction	32-bit pattern and 32-bit mask Up to 15 of each CCSDS (255,223); other options available 5-way interleave depth; other options available
	Encoding Also available	CCSDS (255,223); other options available Shortened codes using virtual fill Randomization/derandomization
Connectors	One 15-pin D	
Cabling	Consult EDT for purchase options.	
Physical	Weight Dimensions	3.1 oz. typical 6.6 x 4.2 x 0.5 in. (with a main board)
Environmental	Temperature Humidity	Operating 0° to 40° C Non-operating -40° to 70° C Operating 1% to 90%, non-condensing at 40° C Non-operating 95%, non-condensing at 45° C
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.	

Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

Contact

Engineering Design Team (EDT), Inc.
1100 NW Compton Drive, Suite 306
Beaverton, Oregon 97006
800-435-4320 / 503-690-1234 (phone)
503-690-1243 (fax)
www.edt.com / info@edt.com

Ordering Options

- Main board: PCI SS / PCI GS / PCIe8 LX
- Clocks: **2 (SSEP)** / 1 (SSE)

Bold is default.
For more options, see main board datasheet.