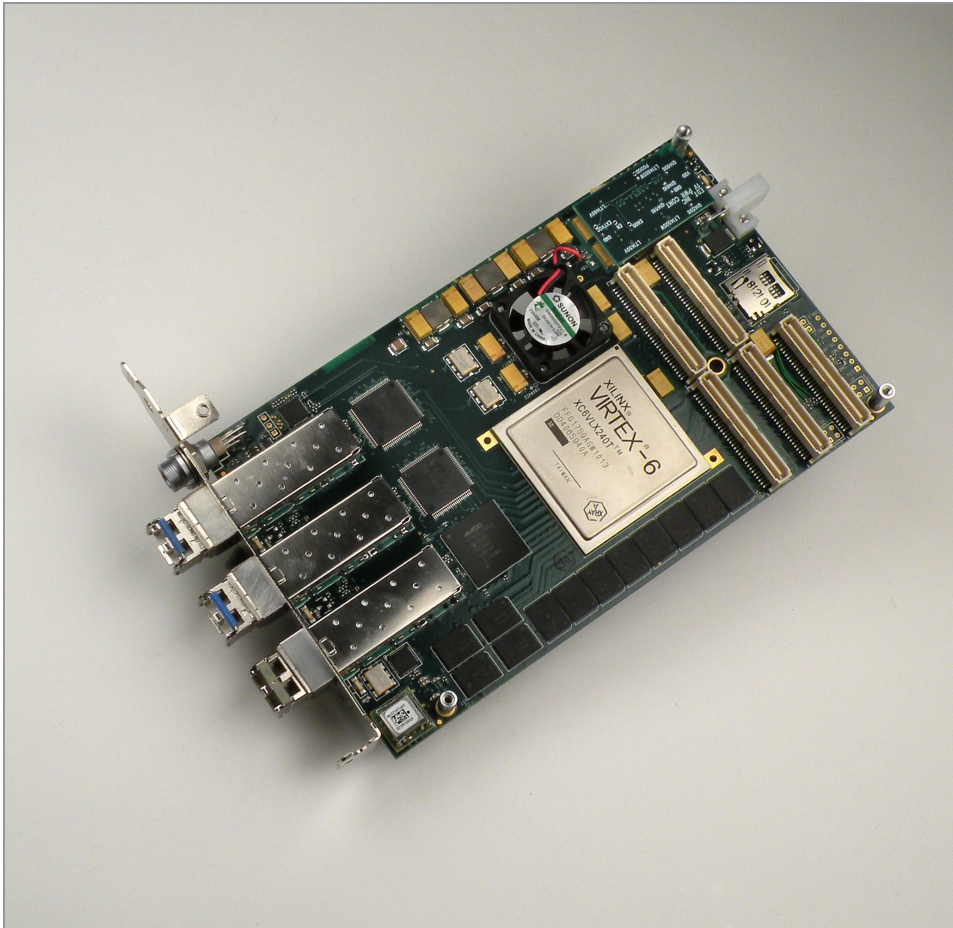


3P

Three-port interface for up to 10GbE / OC192 (STM64) / OTU2f



Description

The 3P is a three-port mezzanine board that pairs with a PCIe main board to provide three independent ports, each supporting one optional transceiver. Port 0 supports an SFP+ for 10GbE (optical), OC192 (STM64), or OTU2/2e/2f; ports 1 and 2 each support an SFP for 1GbE (electrical or optical), OC3/12/48 (STM1/4/16), or OTU1. SDDS data processing is available as an option.

The user-configurable FPGA (Xilinx Virtex 6) can access three independent 512 MB blocks of DDR2 DRAM, which can be used as data buffers. Two of these can be combined to create a memory block of 1GB.

Each port links to a SERDES via a specialized LIU or, optionally, via a multigigabit transceiver (MGT) in the FPGA. Each port has its own reference clock, programmable from 10 to 210 MHz. A time code input (1 pps or IRIG-B) also is included.

EDT provides FPGA configuration files to support 1GbE and 10GbE at the PHY layer; OC3/12/48/192 (raw, framed, framed and descrambled, header, and payload); OTU1/2/2e/2f (raw, framed, framed and descrambled); and demultiplexing. Custom files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Features

Mezzanine board – pairs with an EDT main board (PCIe), which adds DMA, programmable FPGA resources, and memory

Port 0: One optional SFP+ for 10GbE (optical), OC192 (STM64), or OTU2/2e/2f at 1550 or 1310 nm (or 10GbE at 850 nm)

Port 1: One optional SFP for 1GbE (electrical or optical), OC3/12/48 (STM1/4/16), or OTU1 at 1550, 1310, or 850 nm

Port 2: Identical to (but independent of) port 1

Data processing: SDDS (optional)

FPGA: One programmable Xilinx Virtex 6 (XC6VLX240T, LX365T, SX315T, or SX475T)

DRAM (DDR2): Three independent 512 MB blocks (or combine two for 1 GB)

SERDES: Port 0 = 10G LIU or FPGA MGT; port 1 = SONET/SDH LIU or FPGA MGT; port 2 = SONET/SDH LIU or FPGA MGT

EDT intellectual property for 10GbE PCS and PMA layer, SONET/SDH framing, demultiplexing, and G.709 framing

Time code input: 1 pps or IRIG-B, with user-configurable output

Applications

Telecommunications monitoring, recording, and processing

SONET/SDH to ethernet conversion

SDDS data processing

Multiple other network processing applications

Specifications

Product Type	Three-port interface for signals up to 10GbE, OC192 (STM64), or OTU2f; it requires an EDT PCIe main board.			
FPGA Resources	One programmable FPGA (Xilinx Virtex 6 XC6VLX240T, LX365T, SX315T, or SX475T), plus FPGA resources on main board			
Memory	DRAM (DDR2) for snapshot recording / data buffering Three independent 32-bit wide 512 MB blocks; two can be combined into a 64-bit wide 1 GB block			
Clocks	Three (reference) – one per port – independently programmable from 10 to 210 MHz; port 0 has additional jitter attenuation.			
Data Rates	Dependent on such factors as data format, main board, and system variables.			
Data Format (I/O)		Ethernet	SONET (SDH)	ITU-T G.709
	Port 0	10GbE (10G BASE-R)	OC192 (STM64)	OTU2/2e/2f
	Port 1	1GbE (1000 BASE-T or -X)	OC3/12/48 (STM1/4/16)	OTU1
	Port 2	1GbE (1000 BASE-T or -X)	OC3/12/48 (STM1/4/16)	OTU1
	Also provided is a time code input (to connect to an external source) for 1 pps, IRIG-B, or other input, with user-configurable output.			
Data processing	SDDS (optional) is available; with this option, ports 1 and 2 SERDES should be configured for MGT.			
SERDES	The FPGA MGT is capable of line rates of 750 Mb/s to 6.6 Gb/s – or, with 5x digital over sampling, 150 Mb/s to 750 Mb/s.			
	Port 0	10G LIU or optional MGT		
	Port 1	SDH LIU or optional MGT		
	Port 2	SDH LIU or optional MGT		
Transceivers	Three (an optional SFP+ on port 0, and optional SFPs on ports 1 and 2) are available, supporting data as shown below.			
		ELECTRICAL	OPTICAL	
	PORT 0 (1 SFP+, optional)	[none]	10GbE, OC192 (STM64), OTU2/2e/2f	10GbE, OC192 (STM64), OTU2/2e/2f
			1550 nm	850 nm
	Output power	–	0 to +4 dBm	-8.2 to 0.5 dBm
	Center wavelength	–	1530 to 1565 nm	1260 to 1355 nm
	Sensitivity	–	23 dBm	-10.3 dBm
	Maximum input power	–	-7 dBm	0.5 dBm
	Connector	–	LC	LC
	PORTS 1 and 2 (1 SFP each, optional)	1GbE	1GbE, OC3/12/48 (STM1/4/16), OTU1	1GbE, OC3/12/48 (STM1/4/16), OTU1
			1550 nm	850 nm
	Output power	–	-2 to 3 dBm	-9.5 to -3 dBm
	Center wavelength	–	1500 to 1580 nm	1270 to 1360 nm
	Sensitivity	–	-28 dBm	-18 dBm
	Maximum input power	–	-9 dBm	0 dBm
	Connector	RJ45	LC	LC
Connectors	One RJ45 or LC on each transceiver (as shown above), plus one 7-pin Lemo for time code input			
Cabling	To 7-pin Lemo on board, from time code source, via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only); for other cabling, consult EDT.			
Physical	Weight / Dimensions		TBD / 6.6 x 4.2 x 0.75 in. (with a main board)	
Environmental	Temperature (operating / non-operating)		0° to 40° C / -40° to 70° C	
	Humidity (operating / non-operating)		1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C	
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.			

Ordering Options

- Main board: PCIe8 LX / FX / SX
 - FPGA: XC6VLX240T / LX365T / SX315T / SX475T
 - Data processing: SDDS / no SDDS
 - SERDES: [options above]
 - Transceivers: 0 / 1 / 2 / 3 [options above]
 - Cabling (for time code input): DB9 / BNC
- Bold** is default. For more options, see main board detail. **Ask** about custom options.

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