



Komodo Fiber Reference Guide

(Part-No. KY-FGF)

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Revision History

Version	Date	Notes
1.0	30/06/15	Initial Release
1.1	16/07/15	Minor updates

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2.1 Safety Precautions

With your *Komodo Fiber* in hand, please take a minute to read carefully the precautions listed below in order to prevent unnecessary injuries to you or other personnel or cause damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to act upon it to prevent misuse of product.**



Caution

In the event of a failure, disconnect the power supply.

If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.

If an unpleasant smell or smoking occurs, disconnect the power supply.

If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.

Do not disassemble, repair or modify the product.

Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.

Do not touch a cooling fan.

As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.

Do not place the product on unstable locations.

Otherwise, it may drop or fall, resulting in injury to persons or failure.

If the product is dropped or damaged, do not use it as is.

Otherwise, a fire or electric shock may occur.

Do not touch the product with a metallic object.

Otherwise, a fire or electric shock may occur.

Do not place the product in dusty or humid locations or where water may splash.

Otherwise, a fire or electric shock may occur.

Do not get the product wet or touch it with a wet hand.

Otherwise, the product may break down or it may cause a fire, smoking or electric shock.

Do not touch a connector on the product (gold-plated portion).

Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Do not use or place the product in the following locations.

- Humid and dusty locations
- Airless locations such as closet or bookshelf
- Locations which receive oily smoke or steam
- Locations close to heating equipment
- Closed inside of a car where the temperature becomes high
- Static electricity replete locations
- Locations close to water or chemicals

Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.

Do not place heavy things on the product.

Otherwise, the product may be damaged.

Be sure to drain static electricity from body before you touch any electronics component

The electronic circuits in your computer and the circuits on Komodo board are sensitive to static electricity and surges. Improper handling can seriously damage the circuits. In addition, do not let your clothing come in contact with the circuit boards or components.

Otherwise, the product may be damaged.

2.2 Disclaimer

Even if the product is used properly, KAYA Instruments assumes no responsibility for any damages caused by the following:

- Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts caused by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- Secondary impact arising from use of this product or its unusable state (business interruption or others).
- Use of this product against the instructions given in this manual or malfunctions due to connection to other devices. KAYA Instruments assumes no responsibility or liability for:
 - Erasure or corruption of data arising from use of this product.
 - Any consequences or other abnormalities arising from use of this product, or damage of this product not due to our responsibility or failure due to modification.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

3.1 Overview

Komodo Fiber is high-performance yet low-cost FPGA card supporting four SFP+ 10GigE transceivers and a single QSFP 40GigE optical interface. The card is based on Arria V GZ powerful FPGA that offers up to 400K flexible logic elements, 1K DSP blocks and 28Mbit of embedded memory. The board offers a flexible DDR3 memory system with up to 144 Gb of memory and 16 GByte/s throughput. A high speed x8 lane Gen 3.0 PCI express interface allows fast data transfers between optical links and computer memory while a versatile GPIO with multi-standard support enables connection to external devices. The QSFP and SFP interfaces are connected directly to FPGA device transceiver channels to minimize latency.

All of these features combine make the Komodo Fiber ideal for a wide range of applications, including network processing and security, compute and storage, instrumentation, broadcast, defense and aerospace.

3.2 Features

- 4 x SFP+ channels at 10 Gbps each
- 1 x QSFP channel at 40 Gbps
- PCIe Gen3 x8 Half-length card
- Up to 144 Gb of DDR3 memory
 - On-board 16Gb DDR3 64bit wide
 - SODDIMM of up to 128Gb DDR3 64bit wide
 - DDR3 1066 rate compatible
- Altera Arria V GZ FPGA with:
 - 400K equivalent LEs
 - 1092 DSP blocks
 - 28Mbit of embedded memory
 - Hard IP PCIe Gen 3.0 block
- Supports Altera's PCIe IP
- Supports Ethernet IPs
- Supports Memory controller IPs
- Flexible machine I/O:
 - 4 TTL configurable I/Os

- 4 LVCMOS configurable I/Os
- 2 LVDS inputs
- 2 LVDS outputs
- 4 opto-isolated outputs
- 4 opto-isolated inputs
- 2 quadrature rotary encoders
- Integrated strobe controller
- Transfer Rate of up to 60 Gbps through PCIe
- Transfer Rate of up to 80 Gbps through optical interfaces
- CWDM support
- QSFP can be expanded to 4x 10G interfaces
- Temperature control
- Fan control
- 4 indication LEDs
- 0°C to 50°C operating environment temperature

3.3 Product Applications

- Machine Vision
- Networking
- Algorithm Acceleration
- Broadcasting and sports analytics
- High-speed DVRs

3.4 Related documents and accessories

Documents:

- Komodo Fiber Reference Guide
- Reference design

Accessories:

- SFP+ module
- QSFP module
- GPIO extension panel

4.1 Board component Blocks

One Arria V GZ 5AGZME5HF35C4 FPGA in a 1152-pin BGA (FBGA)

- 400K LEs
- 1092 DSP blocks
- 28 Mbit on-die block memory
- 3276 9x9 multipliers
- 2184 18x18 multipliers
- 1092 27x27 multipliers
- 546 36x36 multipliers
- 534 general purpose input/output

FPGA configuration circuitry

- JTAG header
- EPCQ256 programmable flash memory

Clocking circuitry

- Two 322.265625-MHz LVDS oscillator for transceiver reference clock (1 of them is optional)
- 125-MHz LVDS oscillator for transceiver reference clock
- 100-MHz reference clock from the PCIe edge connector
- Two 25-MHz single-ended oscillator for DDR3 memory

Memory

- 16Gb DDR3, 64 bit data width
- up to 128Gb DDR3, 64 bit data width SODIMM (optional)

General user I/O

- Four user LEDs
- GPIO header with up to 20 possible I/O connections

SFP+ and QSFP

- Four SFP+ modules
- One QSFP module
- Four SFP+ interface transmit/receive LED (dual-color)
- Four QSFP interface transmit/receive LED (dual-color)

Power supply

- PCI Express edge connector power

4.2 Board Block diagram

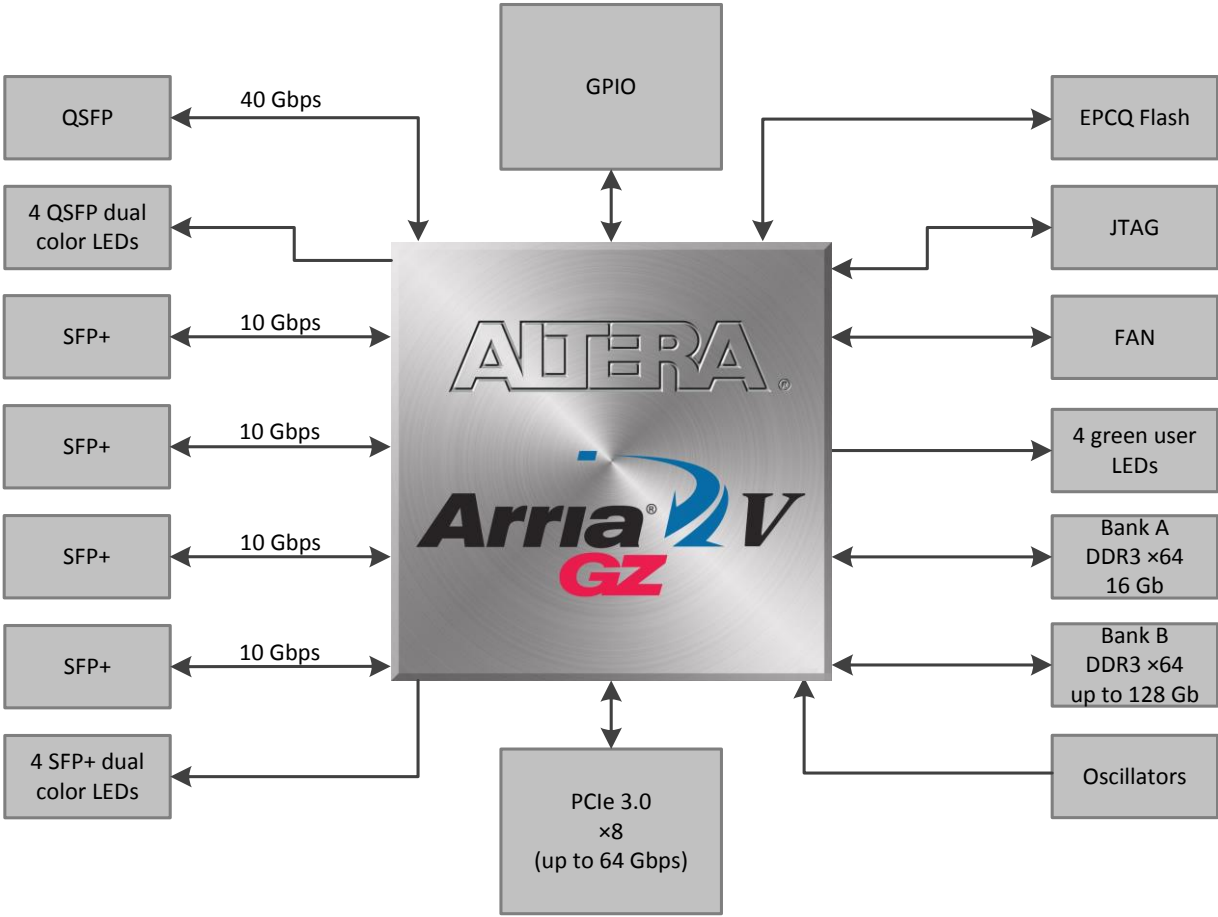


Figure 1: Board block diagram

4.3 External View of the Board

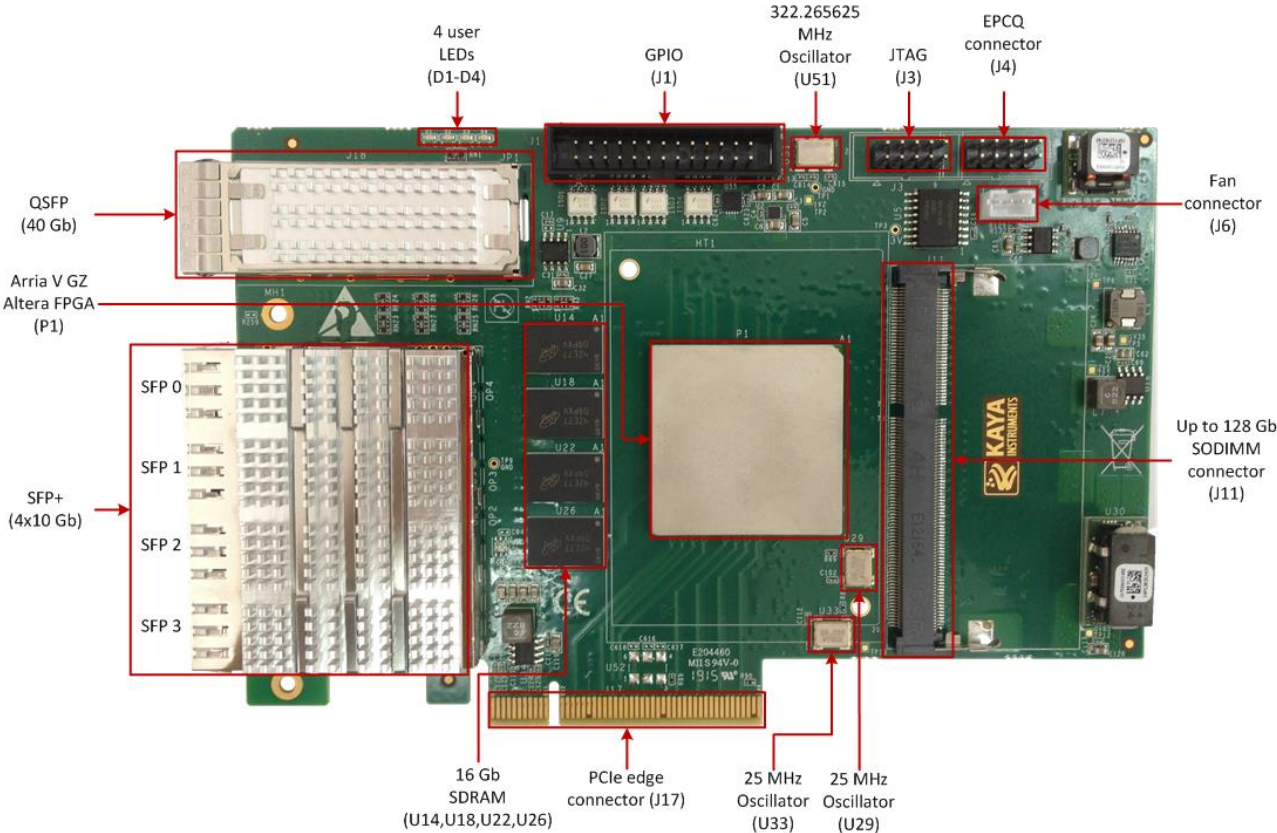


Figure 2: Komodo Fiber front view

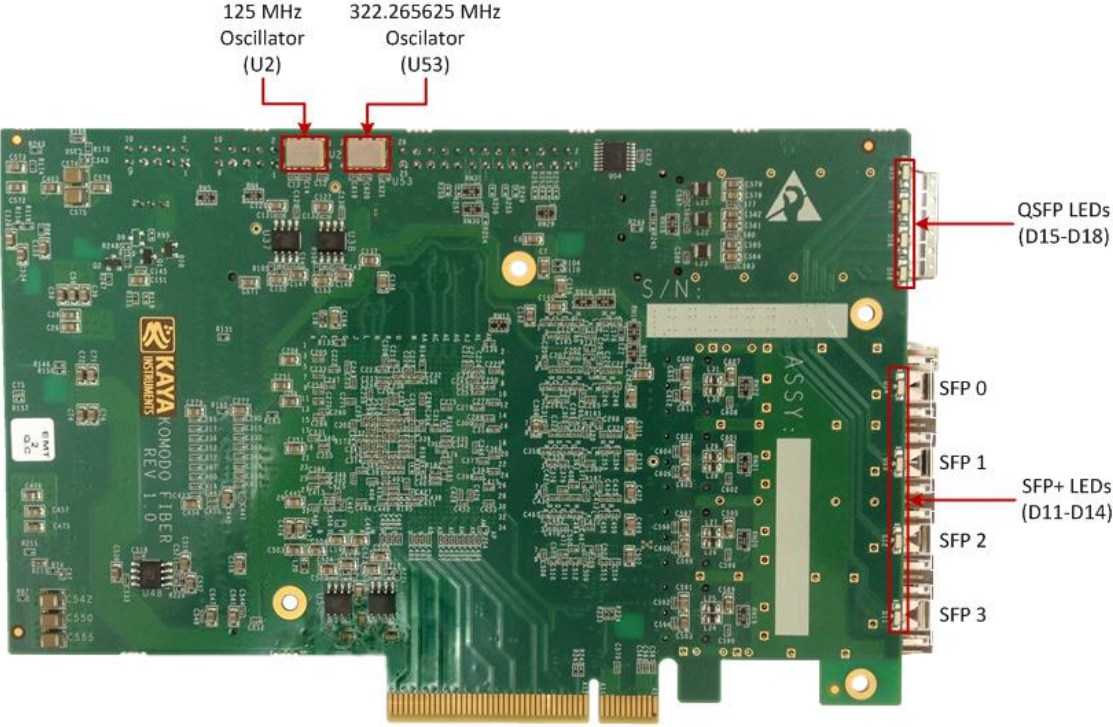


Figure 3: Komodo Fiber back view

4.4 Komodo Fiber Board components

Board reference	Type	Description
FPGA		
P1	FPGA	Arria V GZ 5AGZME5HF35, 1152-pin FBGA
Configuration, Status and setup elements		
J3	JTAG header	Provide access to the JTAG chain
J4	EPCQ programming header	Provide access to the EPCQ using Active Serial protocol
D11 - D14	SFP+ LEDs	Shows transmit or receive activity on SFP+ module
D15 - D18	QSFP LEDs	Shows transmit or receive activity on QSFP module
Clocking Circuitry		
U2	125 MHz oscillator	125 MHz oscillator for transceiver reference clock
J17	100 MHz reference clock	100 MHz reference clock from the PCIe edge connector
U29 , U33	25 MHz oscillator	25 MHz oscillators for DDR3 memory
U51 , U53	322.265625 MHz oscillator	322.265625 MHz oscillators for transceiver reference clock
Memory devices		
U14,U18,U22,U26	DDR3 x64 memory	16Gb DDR3 SDRAM with 64 bit data bus. The 64 bit data bus consists of 4 x16 devices with single address or command bus
J11	DDR3 x64 SODIMM memory	Up to 128Gb DDR3 SODIMM with 64 bit data bus.
General User Input\Output		
D1 - D4	User LEDs	Four user LEDs. Active low.
Communication Ports		
J17	PCIe edge connector	Gold-plated edge fingers connector for up to x8 signaling in Gen 2 or Gen 3
J1	GPIO	General purpose input\output connector
Power supply		
J17	PCIe edge connector	Interface to a PCIe root port such as an appropriate PC motherboard

Table 1: Komodo Fiber board components

4.5 Featured device: Arria V GZ FPGA

The Komodo Fiber features Arria V GZ 5AGZME5HF35 device (P1) in a 1152-pin FBGA package. For more information about Arria V device family refer to [the Arria V device Handbook](#).

4.6 FPGA Configuration

The Komodo Fiber FPGA can be configured using the JTAG header (J3) or by using the on board EPCQ256 Flash that can be programmed using flash programming header (J4) with Active Serial protocol.

4.6.1 FPGA configuration via JTAG

The JTAG programming header provides a method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG header (J3).

4.6.2 FPGA configuration via on board flash memory

The Komodo Fiber has an on board EPCQ256 flash memory. Upon the power up, the FPGA tries to fetch the configuration from that flash. The EPCQ256 flash can be programmed using an external USB-Blaster device with the Quartus II Programmer running on a PC in Active Serial mode. The external USB-Blaster connects to the board through the flash programming header (J4).

4.7 Clocking

The Komodo Fiber has a variety of on board oscillators, as described in the table and figure below:

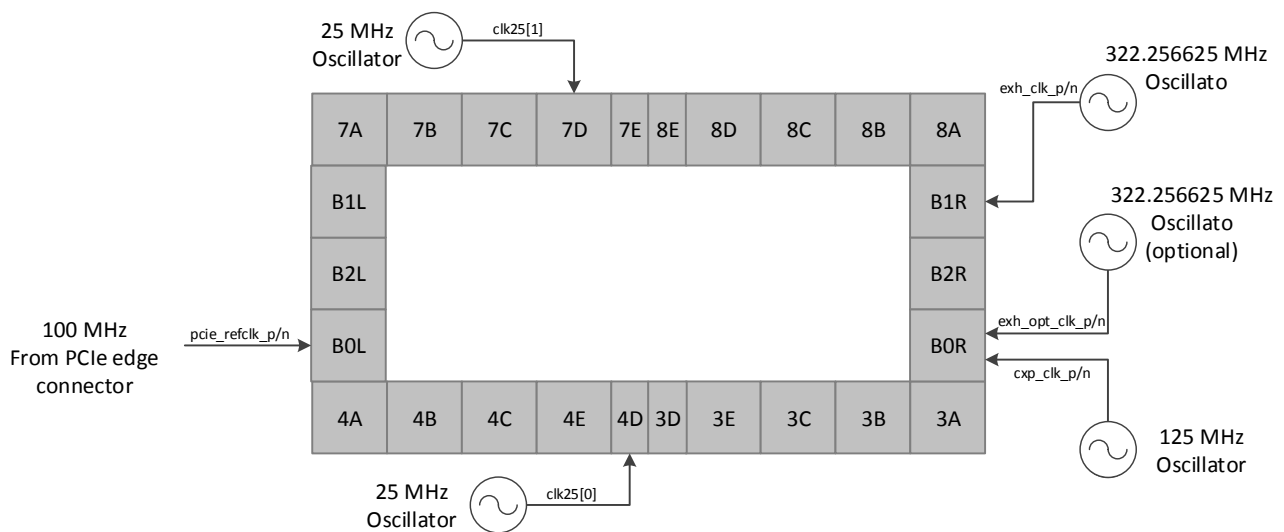


Figure 4: Clocks pin assignments, signal name and functions

Board reference	Signal Name	Arria V GZ Pin Number	Arria V GZ Clock Name	I/O Standard	Description
U2	exp_clkp	W6	REFCLK0Rp	LVDS	125 MHz oscillator for transceiver reference clock
	exp_clkn	W5	REFCLK0Rn		
U29	clk25[0]	AE16	CLK7p	SSTL-135	25 MHz oscillators for DDR3 memory
U33	clk25[1]	J19	CLK19p		
J17	pcie_refclk_p	U28	REFCLK1Lp	HCSL	100 MHz clock coming from the PCI express edge connector
	pcie_refclk_n	U29	REFCLK1Ln		
U51	eth_clkp	R6	REFCLK2Rp	LVDS	322.265625 MHz oscillator for transceiver reference clock
	eth_clkn	R5	REFCLK2Rn		
U52	eth_opt_clkp	U7	REFCLK1Lp	LVDS	Optional 322.265625 MHz oscillators for transceiver reference clock
	eth_opt_clkn	U6	REFCLK1Ln		

Table 2: Clocks pin assignments, signal name and functions

4.8 I/O and Transceivers

The Komodo Fiber utilizes several I/O banks out of the possible 26 I/O or transceiver banks available on the Arria V GZ FPGA. The following figure describes what each bank is used for:

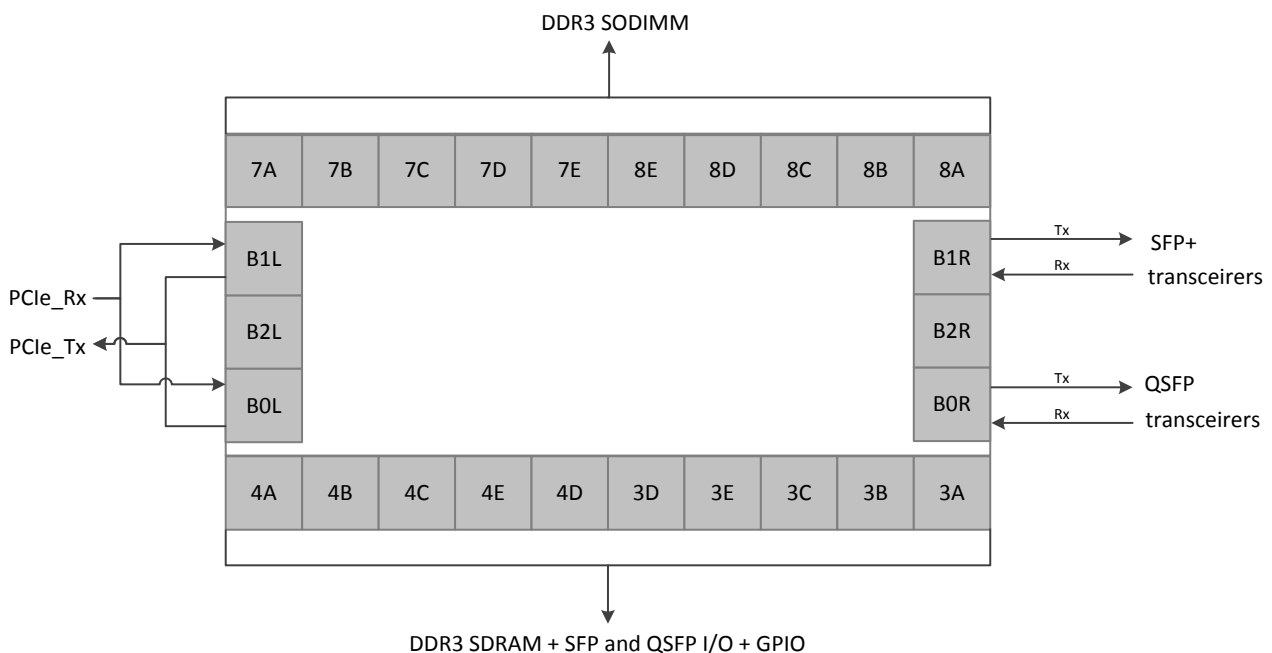


Figure 5: I/O and transceiver usage

4.8.1 General purpose I/O

The Komodo Fiber supports 20 different I/O connections (on the FPGA), as described in Figure 6 and Table 3:

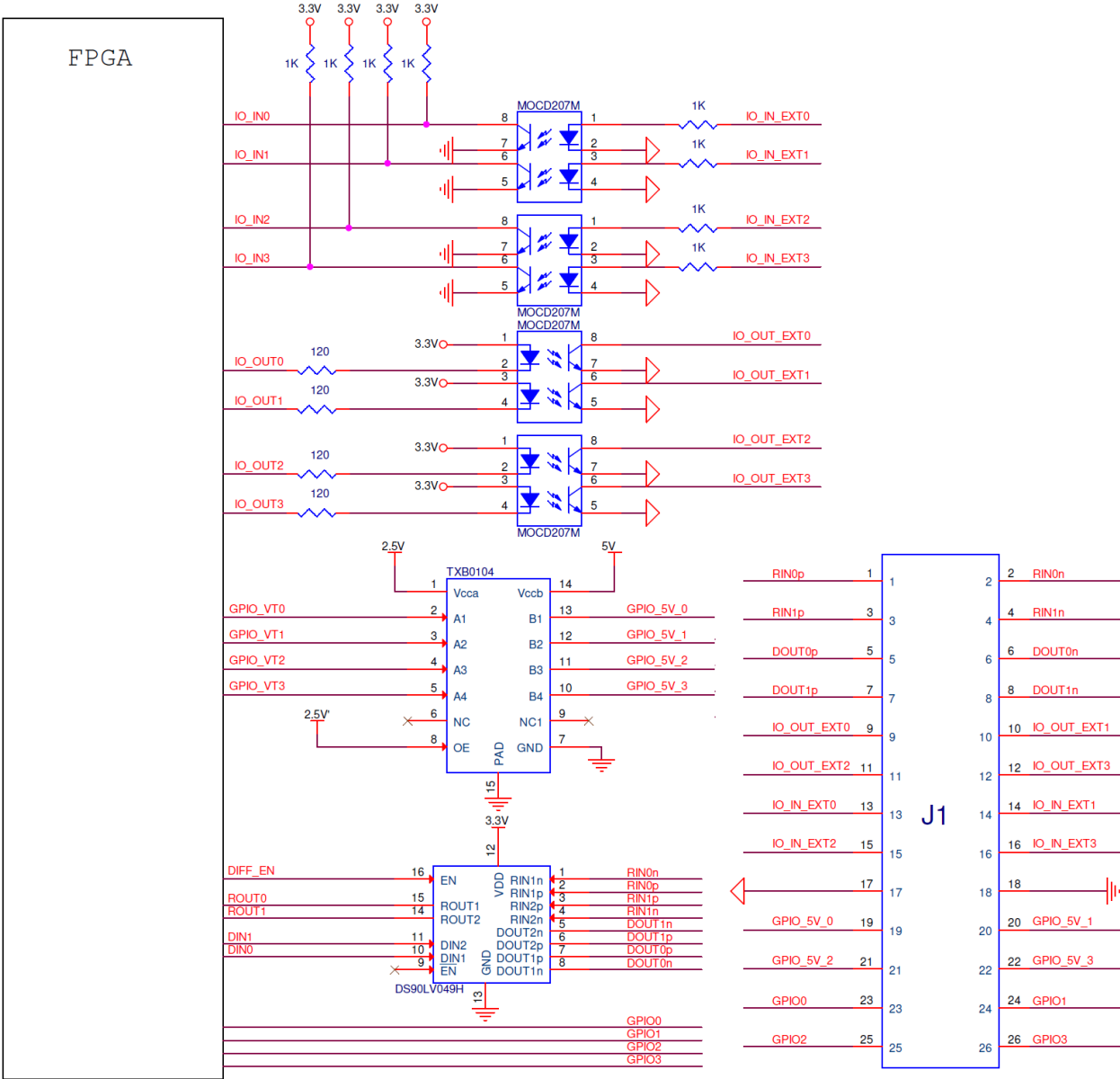


Figure 6: General purpose Inputs and outputs

Board reference (J1)	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
1	rout[0]	AH26	3.3-V LVTTTL	Pin 1 of this header is the positive signal and pin 2 in the negative signal of this LVDS. The differential pair is converted to a single input on the FPGA
2				
3	rout[1]	AK28	3.3-V LVTTTL	Pin 3 of this header is the positive signal and pin 4 in the negative signal of this LVDS. The differential pair is converted to a single input on the FPGA
4				
5	din[0]	AK27	3.3-V LVTTTL	Pin 5 of this header is the positive signal and pin 6 in the negative signal of this LVDS. The differential pair is converted to a single output on the FPGA
6				
7	din[1]	AM26	3.3-V LVTTTL	Pin 7 of this header is the positive signal and pin 8 in the negative signal of this LVDS. The differential pair is converted to a single output on the FPGA
8				
9	io_out[0]	AF26	3.3-V LVTTTL	Optically isolated outputs
10	io_out[1]	AE26	3.3-V LVTTTL	Optically isolated outputs
11	io_out[2]	AD26	3.3-V LVTTTL	Optically isolated outputs
12	io_out[3]	AC26	3.3-V LVTTTL	Optically isolated outputs
13	io_in[0]	U26	3.3-V LVTTTL	Optically isolated inputs
14	io_in[1]	Y25	3.3-V LVTTTL	Optically isolated inputs
15	io_in[2]	W25	3.3-V LVTTTL	Optically isolated inputs
16	io_in[3]	V25	3.3-V LVTTTL	Optically isolated inputs
17	OptoCoupled GND	-	-	Ground signal for opto-isolated signals on this connector
18	GND	-	-	Reference ground signal - Board GND
19	gpio_vt[0]	AM11	TTL	General Purpose IO
20	gpio_vt[1]	AL11	TTL	
21	gpio_vt[2]	AM10	TTL	
22	gpio_vt[3]	AL10	TTL	
23	gpio[0]	AA30	3.3-V LVTTTL	
24	gpio[1]	AE28	3.3-V LVTTTL	
25	gpio[2]	AD28	3.3-V LVTTTL	
26	gpio[3]	AB27	3.3-V LVTTTL	

Table 3: General purpose Inputs and outputs pin assignments, signal name and functions

The “diff_en” signal coming from the FPGA, enables (when set to logic 1) data transfer from pins 1 - 4 on the GPIO header, to pins AH26 and AK28 on the FPGA. This signal also enables data transfer from pins AK27 and AM26 on the FPGA to pins 5 – 8 on the GPIO header.

4.8.2 General purpose LEDs

On the Komodo Fiber there are four user-define LEDs, all are green light and active low.

Board reference	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
D1	led[0]	AB11	2.5 V (Open drain)	User-defined LEDs. Driving logic 0 on the I\O port turns the LED on; driving high-z on the I\O turns the LED off
D2	led[1]	AE10	2.5 V (Open drain)	
D3	led[2]	AE11	2.5 V (Open drain)	
D4	led[3]	W11	2.5 V (Open drain)	

Table 4: General purpose LEDs pin assignments, signal name and functions

4.9 PCI Express (Gen 3.0)

The Komodo Fiber is designed to fit entirely into a PC motherboard with a ×8 PCI Express slot that can accommodate a full height long form factor add-in card.

The PCI Express edge connector has a connection speed of 2.5 Gbps/lane for a maximum of 20 Gbps full-duplex (Gen1) or 5.0 Gbps/lane for a maximum of 40 Gbps full-duplex (Gen2) or 8.0 Gbps/lane for a maximum of 64 Gbps full-duplex (Gen3).

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard.

The PCIe reference clock is a 100 MHz differential input that is driven from the PC motherboard on to this board through the edge connector. This clock is connected directly to an Arria V GZ refclk input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required.

JTAG signals (TCK, TDI, TDO and TMS) of the PCIe connector are not connected to the FPGA.

Board reference (J17)	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
A1	pcie_prsntn1n	-	3.3-V LVTTL	Hot plug presence detect
B17	pcie_prsntn1n_x1	-	3.3-V LVTTL	Hot plug presence detect
B31	pcie_prsntn1n_x4	-	3.3-V LVTTL	Hot plug presence detect
B48	pcie_prsntn1n_x8	-	3.3-V LVTTL	Hot plug presence detect
A5	pcie_jtag_tck	-	3.3-V LVTTL	JTAG chain clock
A6	pcie_jtag_tdi	-	3.3-V LVTTL	JTAG chain data in
A7	pcie_jtag_tdo	-	3.3-V LVTTL	JTAG chain data out

A8	pcie_jtag_tms	-	3.3-V LVTTL	JTAG chain mode select
A13	pcie_refclk_p	U28	HCSL	Motherboard reference clock (P)
A14	pcie_refclk_n	U29	HCSL	Motherboard reference clock (N)
A11	pcie_perstn	W26	3.3-V LVTTL	Reset
B11	pcie_waken	W24	3.3-V LVTTL	Wake signal
B6	pcie_smbdat	V24	3.3-V LVTTL	SMB data
B5	pcie_smbclk	AA24	3.3-V LVTTL	SMB clock
A16	pcie_tx_p[0]	AK31	1.5-V PCML	Transmit bus
A17	pcie_tx_n[0]	AK32	1.5-V PCML	
A21	pcie_tx_p[1]	AH31	1.5-V PCML	
A22	pcie_tx_n[1]	AH32	1.5-V PCML	
A25	pcie_tx_p[2]	AF31	1.5-V PCML	
A26	pcie_tx_n[2]	AF32	1.5-V PCML	
A29	pcie_tx_p[3]	AD31	1.5-V PCML	
A30	pcie_tx_n[3]	AD32	1.5-V PCML	
A35	pcie_tx_p[4]	Y31	1.5-V PCML	
A36	pcie_tx_n[4]	Y32	1.5-V PCML	
A39	pcie_tx_p[5]	V31	1.5-V PCML	
A40	pcie_tx_n[5]	V32	1.5-V PCML	
A43	pcie_tx_p[6]	T31	1.5-V PCML	
A44	pcie_tx_n[6]	T32	1.5-V PCML	
A47	pcie_tx_p[7]	P31	1.5-V PCML	
A48	pcie_tx_n[7]	P32	1.5-V PCML	
B14	pcie_rx_p[0]	AL33	1.5-V PCML	
B15	pcie_rx_n[0]	AL34	1.5-V PCML	
B19	pcie_rx_p[1]	AJ33	1.5-V PCML	
B20	pcie_rx_n[1]	AJ34	1.5-V PCML	
B23	pcie_rx_p[2]	AG33	1.5-V PCML	
B24	pcie_rx_n[2]	AG34	1.5-V PCML	
B27	pcie_rx_p[3]	AE33	1.5-V PCML	
B28	pcie_rx_n[3]	AE34	1.5-V PCML	
B33	pcie_rx_p[4]	AA33	1.5-V PCML	
B34	pcie_rx_n[4]	AA34	1.5-V PCML	
B37	pcie_rx_p[5]	W33	1.5-V PCML	
B38	pcie_rx_n[5]	W34	1.5-V PCML	
B41	pcie_rx_p[6]	U33	1.5-V PCML	
B42	pcie_rx_n[6]	U34	1.5-V PCML	
B45	pcie_rx_p[7]	R33	1.5-V PCML	
B46	pcie_rx_n[7]	R34	1.5-V PCML	

Table 5: PCIe pin assignments, signal name and functions

4.10 Memory

On the Komodo Fiber there are 2 memory interfaces, this section describes those interfaces and also signal names, types, and connectivity relative to the Arria V GZ. The starter board has the following memory interfaces:

- 16Gb DDR3 on-board SDRAM with 64bit data width, 1066 rate compatible.
- Up to 128Gb DDR3 SODIMM with 64bit data width, 1066 rate compatible (J11).

If any, or both, of those memories are used, the RZQ signal must be connected to the DDR3 control IP. If only the on-board DDR3 memory is used, this signal should be connected to the DDR3 IP that controls this memory, as shown in Figure 7:

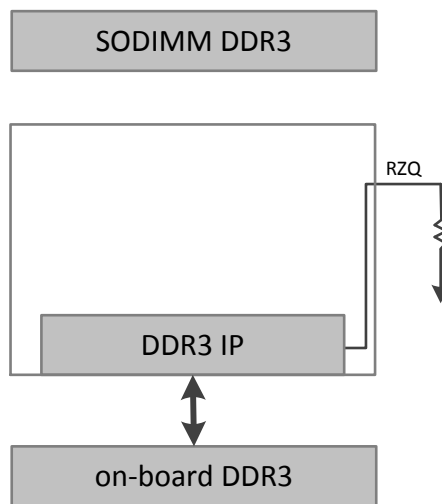


Figure 7: RZQ connection when only the on-board memory is used

If only the SODIMM DDR3 memory is used, this signal should be connected to the DDR3 IP that controls this memory, as shown in Figure 8:

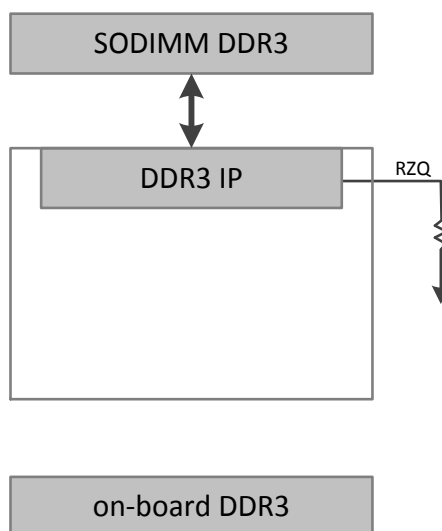


Figure 8: RZQ connection when only the SODIMM memory is used

If both memories are used, the RZQ signal must be connected to both of the DDR3 controller. Both controllers must have “sharing” enabled. One controller must be configured as master, this is done by selecting “Master” in the “PHY Settings” tap, under “Advanced PHY Settings”, in the “OCT sharing mode” selection. The other DDR3 controller must be configured as a slave (the same way as the first one was configured as a master, but the “OCT sharing mode” should be “Slave”). The RZQ signal is connected to the master DDR3 controller and the through it also connected to the slave DDR3 controller, as shown in Figure 9:

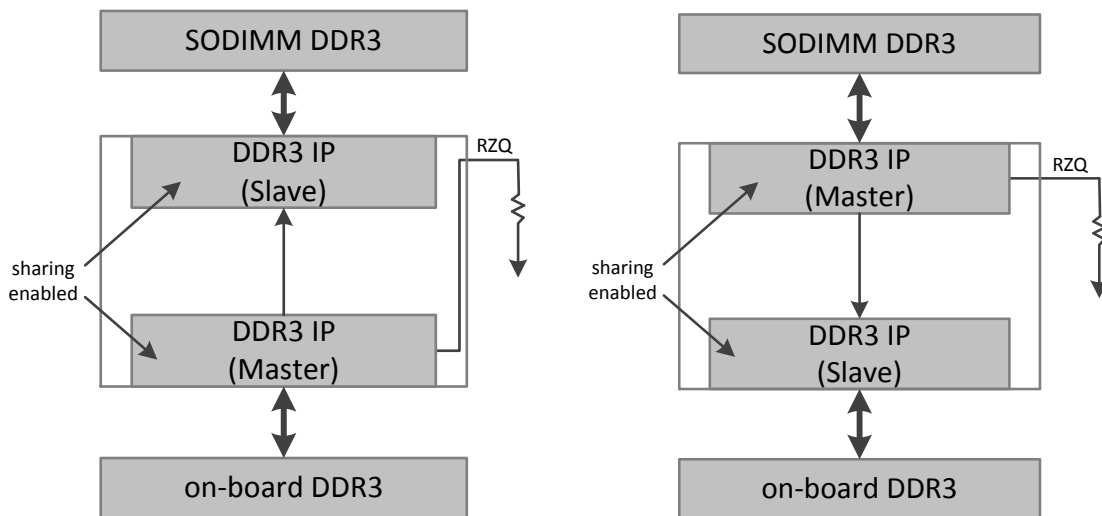


Figure 9: RZQ connection when both memories are used

4.10.1 On-Board 16Gb DDR3

The Komodo Fiber supports four, 32Mx16x8 bank, DDR3 SDRAM interface for very high-speed sequential memory access. The 64-bit data bus consists of four x16 devices with a single address or command bus. This interface support rates of up to 1066 MT/s. This interface connects to the vertical I/O banks on the top edge of the FPGA.

The four x16 devices share some of the control signals, in the following Figure 10 and Table 6 those signals are shown:

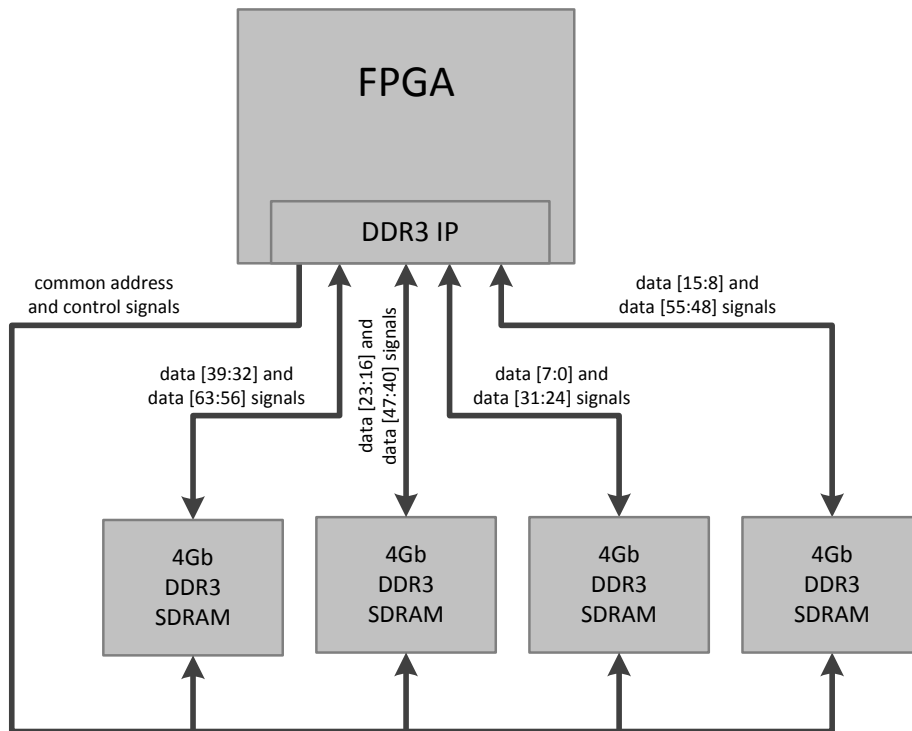


Figure 10: On-board DDR3 signal connections

Board reference	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
Common control signals to all four on-board SDRAMs				
N3	ddr3_2_a[0]	AC14	1.35-V SSTL	Address bus
P7	ddr3_2_a[1]	AD15	1.35-V SSTL	
P3	ddr3_2_a[2]	W21	1.35-V SSTL	
N2	ddr3_2_a[3]	AG12	1.35-V SSTL	
P8	ddr3_2_a[4]	AN21	1.35-V SSTL	
P2	ddr3_2_a[5]	U22	1.35-V SSTL	
R8	ddr3_2_a[6]	AC15	1.35-V SSTL	
R2	ddr3_2_a[7]	AF15	1.35-V SSTL	
T8	ddr3_2_a[8]	AF12	1.35-V SSTL	
R3	ddr3_2_a[9]	AB12	1.35-V SSTL	
L7	ddr3_2_a[10]	AG13	1.35-V SSTL	
R7	ddr3_2_a[11]	AN18	1.35-V SSTL	
N7	ddr3_2_a[12]	AF11	1.35-V SSTL	
T3	ddr3_2_a[13]	AF14	1.35-V SSTL	
T7	ddr3_2_a[14]	AJ12	1.35-V SSTL	
M7	ddr3_2_a[15]	AH14	1.35-V SSTL	
M2	ddr3_2_ba[0]	AE23	1.35-V SSTL	Bank address bus
N8	ddr3_2_ba[1]	AH13	1.35-V SSTL	

M3	ddr3_2_ba[2]	AA15	1.35-V SSTL	
K9	ddr3_2_cke	W19	1.35-V SSTL	Clock enable
J7	ddr3_2_clk_p	AE14	Differential 1.35-V SSTL	Differential clock input
K7	ddr3_2_clk_n	AE13	Differential 1.35-V SSTL	
L2	ddr3_2_csn	AH15	1.35-V SSTL	Chip select
L3	ddr3_2_wen	AD14	1.35-V SSTL	Write enable
J3	ddr3_2_rasn	AB15	1.35-V SSTL	Row address select
K3	ddr3_2_casn	AA12	1.35-V SSTL	Column address select
T2	ddr3_2_resetn	AM13	1.35-V SSTL	reset
K1	ddr3_2_odt	AH12	1.35-V SSTL	On-die termination input
DDR3 x16 (U14)				
E7	ddr3_2_dm[7]	AC17	1.35-V SSTL	Write mask byte lane 0
D3	ddr3_2_dm[4]	AJ15	1.35-V SSTL	Write mask byte lane 1
C3	ddr3_2_dq[32]	AK16	1.35-V SSTL	Data bus
D7	ddr3_2_dq[33]	AP16	1.35-V SSTL	
A2	ddr3_2_dq[34]	AH17	1.35-V SSTL	
C8	ddr3_2_dq[35]	AN16	1.35-V SSTL	
B8	ddr3_2_dq[36]	AP15	1.35-V SSTL	
A3	ddr3_2_dq[37]	AK15	1.35-V SSTL	
C2	ddr3_2_dq[38]	AJ17	1.35-V SSTL	
A7	ddr3_2_dq[39]	AN15	1.35-V SSTL	
H3	ddr3_2_dq[56]	AD16	1.35-V SSTL	
F2	ddr3_2_dq[57]	W15	1.35-V SSTL	
G2	ddr3_2_dq[58]	W16	1.35-V SSTL	
F7	ddr3_2_dq[59]	AG16	1.35-V SSTL	
H8	ddr3_2_dq[60]	W17	1.35-V SSTL	
F8	ddr3_2_dq[61]	Y16	1.35-V SSTL	
H7	ddr3_2_dq[62]	AG15	1.35-V SSTL	
E3	ddr3_2_dq[63]	AD17	1.35-V SSTL	
F3	ddr3_2_dqs_p[7]	AF16	Differential 1.35-V SSTL	Data strobe P byte lane 0
G3	ddr3_2_dqs_n[7]	AF17	Differential 1.35-V SSTL	Data strobe N byte lane 0
C7	ddr3_2_dqs_p[4]	AM16	Differential 1.35-V SSTL	Data strobe P byte lane 1
B7	ddr3_2_dqs_n[4]	AL16	Differential 1.35-V SSTL	Data strobe N byte lane 1
DDR3 x16 (U18)				
E7	ddr3_2_dm[2]	AL19	1.35-V SSTL	Write mask byte lane 0
D3	ddr3_2_dm[5]	AN22	1.35-V SSTL	Write mask byte lane 1
E3	ddr3_2_dq[16]	AL17	1.35-V SSTL	Data bus
H3	ddr3_2_dq[17]	AM17	1.35-V SSTL	
H8	ddr3_2_dq[18]	AK19	1.35-V SSTL	
F7	ddr3_2_dq[19]	AP18	1.35-V SSTL	
F8	ddr3_2_dq[20]	AG19	1.35-V SSTL	
F2	ddr3_2_dq[21]	AH18	1.35-V SSTL	
H7	ddr3_2_dq[22]	AM18	1.35-V SSTL	
G2	ddr3_2_dq[23]	AJ18	1.35-V SSTL	
C2	ddr3_2_dq[40]	AK22	1.35-V SSTL	
A7	ddr3_2_dq[41]	AL22	1.35-V SSTL	

C8	ddr3_2_dq[42]	AM22	1.35-V SSTL		
C3	ddr3_2_dq[43]	AM20	1.35-V SSTL		
D7	ddr3_2_dq[44]	AP22	1.35-V SSTL		
A3	ddr3_2_dq[45]	AM19	1.35-V SSTL		
A2	ddr3_2_dq[46]	AK21	1.35-V SSTL		
B8	ddr3_2_dq[47]	AP21	1.35-V SSTL		
F3	ddr3_2_dqs_p[2]	AK17	Differential 1.35-V SSTL	Data strobe P byte lane 0	
G3	ddr3_2_dqs_n[2]	AK18	Differential 1.35-V SSTL	Data strobe N byte lane 0	
C7	ddr3_2_dqs_p[5]	AN19	Differential 1.35-V SSTL	Data strobe P byte lane 1	
B7	ddr3_2_dqs_n[5]	AP19	Differential 1.35-V SSTL	Data strobe N byte lane 1	
DDR3 x16 (U22)					
E7	ddr3_2_dm[3]	Y17	1.35-V SSTL	Write mask byte lane 0	
D3	ddr3_2_dm[0]	AH22	1.35-V SSTL	Write mask byte lane 1	
B8	ddr3_2_dq[0]	AF23	1.35-V SSTL	Data bus	
A3	ddr3_2_dq[1]	AJ21	1.35-V SSTL		
C3	ddr3_2_dq[2]	AH20	1.35-V SSTL		
A7	ddr3_2_dq[3]	AG22	1.35-V SSTL		
C8	ddr3_2_dq[4]	AF22	1.35-V SSTL		
C2	ddr3_2_dq[5]	AK20	1.35-V SSTL		
A2	ddr3_2_dq[6]	AJ20	1.35-V SSTL		
D7	ddr3_2_dq[7]	AH23	1.35-V SSTL		
G2	ddr3_2_dq[24]	AF18	1.35-V SSTL		
H8	ddr3_2_dq[25]	W18	1.35-V SSTL		
E3	ddr3_2_dq[26]	AF19	1.35-V SSTL		
F2	ddr3_2_dq[27]	AG18	1.35-V SSTL		
F7	ddr3_2_dq[28]	AA18	1.35-V SSTL		
H7	ddr3_2_dq[29]	Y18	1.35-V SSTL		
H3	ddr3_2_dq[30]	AE19	1.35-V SSTL		
F8	ddr3_2_dq[31]	Y19	1.35-V SSTL		
F3	ddr3_2_dqs_p[3]	AB18	Differential 1.35-V SSTL		Data strobe P byte lane 0
G3	ddr3_2_dqs_n[3]	AB19	Differential 1.35-V SSTL		Data strobe N byte lane 0
C7	ddr3_2_dqs_p[0]	AG21	Differential 1.35-V SSTL	Data strobe P byte lane 1	
B7	ddr3_2_dqs_n[0]	AH21	Differential 1.35-V SSTL	Data strobe N byte lane 1	
DDR3 x16 (U26)					
E7	ddr3_2_dm[1]	Y21	1.35-V SSTL	Write mask byte lane 0	
D3	ddr3_2_dm[6]	W22	1.35-V SSTL	Write mask byte lane 1	
F8	ddr3_2_dq[8]	W20	1.35-V SSTL	Data bus	
H3	ddr3_2_dq[9]	AE20	1.35-V SSTL		
H8	ddr3_2_dq[10]	AA20	1.35-V SSTL		
H7	ddr3_2_dq[11]	AB20	1.35-V SSTL		
F2	ddr3_2_dq[12]	AF21	1.35-V SSTL		
F7	ddr3_2_dq[13]	AA21	1.35-V SSTL		
E3	ddr3_2_dq[14]	AD20	1.35-V SSTL		
G2	ddr3_2_dq[15]	AF20	1.35-V SSTL		
A2	ddr3_2_dq[48]	AD22	1.35-V SSTL		
C2	ddr3_2_dq[49]	AE22	1.35-V SSTL		
A3	ddr3_2_dq[50]	AC23	1.35-V SSTL		

C8	ddr3_2_dq[51]	Y23	1.35-V SSTL	
B8	ddr3_2_dq[52]	V22	1.35-V SSTL	
C3	ddr3_2_dq[53]	AD23	1.35-V SSTL	
D7	ddr3_2_dq[54]	Y22	1.35-V SSTL	
A7	ddr3_2_dq[55]	AA22	1.35-V SSTL	
F3	ddr3_2_dqs_p[1]	AC20	Differential 1.35-V SSTL	Data strobe P byte lane 0
G3	ddr3_2_dqs_n[1]	AC21	Differential 1.35-V SSTL	Data strobe N byte lane 0
C7	ddr3_2_dqs_p[6]	AB21	Differential 1.35-V SSTL	Data strobe P byte lane 1
B7	ddr3_2_dqs_n[6]	AB22	Differential 1.35-V SSTL	Data strobe N byte lane 1

Table 6: On board SDRAM pin assignments, signal name and functions

For more information about the on board SDRAM (MT41K256M16HA-125E) refer to the [MICRON DDR3L SDRAM datasheet](#).

4.10.2 Optional SODIMM (up to 128Gb)

The Komodo Fiber can support up to 128Gb, DDR3 SDRAM interfaces over SODIMM interface for very high-speed sequential memory access. The 64-bit data bus can consist of several x16 devices with a single address or command bus. This interface support rates of up to 1066 MT/s. This interface connects to the vertical I/O banks on the top edge of the FPGA.

Board reference (J11)	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
98	ddr3_1_a[0]	J29	1.35-V SSTL	Address bus
97	ddr3_1_a[1]	P11	1.35-V SSTL	
96	ddr3_1_a[2]	J21	1.35-V SSTL	
95	ddr3_1_a[3]	E13	1.35-V SSTL	
92	ddr3_1_a[4]	K21	1.35-V SSTL	
91	ddr3_1_a[5]	G20	1.35-V SSTL	
90	ddr3_1_a[6]	M12	1.35-V SSTL	
86	ddr3_1_a[7]	N26	1.35-V SSTL	
89	ddr3_1_a[8]	L28	1.35-V SSTL	
85	ddr3_1_a[9]	J20	1.35-V SSTL	
107	ddr3_1_a[10]	F15	1.35-V SSTL	
84	ddr3_1_a[11]	N13	1.35-V SSTL	
83	ddr3_1_a[12]	G21	1.35-V SSTL	
119	ddr3_1_a[13]	E14	1.35-V SSTL	
80	ddr3_1_a[14]	L11	1.35-V SSTL	
78	ddr3_1_a[15]	C23	1.35-V SSTL	Bank address bus
109	ddr3_1_ba[0]	F21	1.35-V SSTL	
108	ddr3_1_ba[1]	F14	1.35-V SSTL	
79	ddr3_1_ba[2]	D16	1.35-V SSTL	
73	ddr3_1_cke[0]	H23	1.35-V SSTL	Clock enable 0
74	ddr3_1_cke[1]	N11	1.35-V SSTL	Clock enable 1
101	ddr3_1_clk_p[0]	E21	Differential 1.35-V SSTL	Differential clock input 0

103	ddr3_1_clk_n[0]	D21	Differential 1.35-V SSTL	Differential clock input 1
102	ddr3_1_clk_p[1]	F20	Differential 1.35-V SSTL	
104	ddr3_1_clk_n[1]	E20	Differential 1.35-V SSTL	
114	ddr3_1_csn[0]	G15	1.35-V SSTL	Chip select 0
121	ddr3_1_csn[1]	B20	1.35-V SSTL	Chip select 1
113	ddr3_1_wen	D13	1.35-V SSTL	Write enable
110	ddr3_1_rasn	H20	1.35-V SSTL	Row address select
115	ddr3_1_casn	C28	1.35-V SSTL	Column address select
30	ddr3_1_resetn	C33	1.35-V SSTL	reset
116	ddr3_1_odt[0]	J22	1.35-V SSTL	On-die termination input 0
120	ddr3_1_odt[1]	N12	1.35-V SSTL	On-die termination input 1
170	ddr3_1_dm[0]	K28	1.35-V SSTL	Write mask byte 0
11	ddr3_1_dm[1]	F18	1.35-V SSTL	Write mask byte 1
187	ddr3_1_dm[2]	P25	1.35-V SSTL	Write mask byte 2
28	ddr3_1_dm[3]	F23	1.35-V SSTL	Write mask byte 3
153	ddr3_1_dm[4]	E27	1.35-V SSTL	Write mask byte 4
46	ddr3_1_dm[5]	D19	1.35-V SSTL	Write mask byte 5
63	ddr3_1_dm[6]	D22	1.35-V SSTL	Write mask byte 6
136	ddr3_1_dm[7]	F27	1.35-V SSTL	Write mask byte 7
177	ddr3_1_dq[0]	J27	1.35-V SSTL	Data bus
163	ddr3_1_dq[1]	L27	1.35-V SSTL	
176	ddr3_1_dq[2]	M27	1.35-V SSTL	
165	ddr3_1_dq[3]	K27	1.35-V SSTL	
174	ddr3_1_dq[4]	L29	1.35-V SSTL	
166	ddr3_1_dq[5]	H25	1.35-V SSTL	
164	ddr3_1_dq[6]	G25	1.35-V SSTL	
175	ddr3_1_dq[7]	J28	1.35-V SSTL	
5	ddr3_1_dq[8]	J18	1.35-V SSTL	
7	ddr3_1_dq[9]	J16	1.35-V SSTL	
17	ddr3_1_dq[10]	F17	1.35-V SSTL	
16	ddr3_1_dq[11]	E17	1.35-V SSTL	
4	ddr3_1_dq[12]	K16	1.35-V SSTL	
15	ddr3_1_dq[13]	G17	1.35-V SSTL	
6	ddr3_1_dq[14]	H17	1.35-V SSTL	
18	ddr3_1_dq[15]	E18	1.35-V SSTL	
194	ddr3_1_dq[16]	M26	1.35-V SSTL	
183	ddr3_1_dq[17]	L26	1.35-V SSTL	
182	ddr3_1_dq[18]	K24	1.35-V SSTL	
191	ddr3_1_dq[19]	P26	1.35-V SSTL	
193	ddr3_1_dq[20]	L24	1.35-V SSTL	
180	ddr3_1_dq[21]	J24	1.35-V SSTL	
181	ddr3_1_dq[22]	K25	1.35-V SSTL	
192	ddr3_1_dq[23]	L25	1.35-V SSTL	
23	ddr3_1_dq[24]	L22	1.35-V SSTL	
33	ddr3_1_dq[25]	H22	1.35-V SSTL	
35	ddr3_1_dq[26]	G22	1.35-V SSTL	
22	ddr3_1_dq[27]	M23	1.35-V SSTL	

34	ddr3_1_dq[28]	E22	1.35-V SSTL	
24	ddr3_1_dq[29]	M22	1.35-V SSTL	
21	ddr3_1_dq[30]	M24	1.35-V SSTL	
36	ddr3_1_dq[31]	G23	1.35-V SSTL	
158	ddr3_1_dq[32]	B28	1.35-V SSTL	
147	ddr3_1_dq[33]	A26	1.35-V SSTL	
148	ddr3_1_dq[34]	A25	1.35-V SSTL	
157	ddr3_1_dq[35]	D28	1.35-V SSTL	
149	ddr3_1_dq[36]	A28	1.35-V SSTL	
160	ddr3_1_dq[37]	B25	1.35-V SSTL	
159	ddr3_1_dq[38]	D27	1.35-V SSTL	
146	ddr3_1_dq[39]	C25	1.35-V SSTL	
40	ddr3_1_dq[40]	A16	1.35-V SSTL	
50	ddr3_1_dq[41]	A20	1.35-V SSTL	
41	ddr3_1_dq[42]	A17	1.35-V SSTL	
39	ddr3_1_dq[43]	B17	1.35-V SSTL	
52	ddr3_1_dq[44]	A19	1.35-V SSTL	
53	ddr3_1_dq[45]	B19	1.35-V SSTL	
51	ddr3_1_dq[46]	C19	1.35-V SSTL	
42	ddr3_1_dq[47]	C17	1.35-V SSTL	
69	ddr3_1_dq[48]	C22	1.35-V SSTL	
67	ddr3_1_dq[49]	A21	1.35-V SSTL	
59	ddr3_1_dq[50]	C21	1.35-V SSTL	
68	ddr3_1_dq[51]	D24	1.35-V SSTL	
56	ddr3_1_dq[52]	A22	1.35-V SSTL	
58	ddr3_1_dq[53]	B22	1.35-V SSTL	
57	ddr3_1_dq[54]	E23	1.35-V SSTL	
70	ddr3_1_dq[55]	E24	1.35-V SSTL	
141	ddr3_1_dq[56]	E26	1.35-V SSTL	
143	ddr3_1_dq[57]	F26	1.35-V SSTL	
129	ddr3_1_dq[58]	H28	1.35-V SSTL	
142	ddr3_1_dq[59]	E28	1.35-V SSTL	
132	ddr3_1_dq[60]	G24	1.35-V SSTL	
140	ddr3_1_dq[61]	H29	1.35-V SSTL	
131	ddr3_1_dq[62]	G28	1.35-V SSTL	
130	ddr3_1_dq[63]	F24	1.35-V SSTL	
171	ddr3_1_dqs_p[0]	G26	Differential 1.35-V SSTL	Data strobe P byte 0
169	ddr3_1_dqs_n[0]	G27	Differential 1.35-V SSTL	Data strobe N byte 0
12	ddr3_1_dqs_p[1]	H19	Differential 1.35-V SSTL	Data strobe P byte 1
10	ddr3_1_dqs_n[1]	G19	Differential 1.35-V SSTL	Data strobe N byte 1
188	ddr3_1_dqs_p[2]	J25	Differential 1.35-V SSTL	Data strobe P byte 2
186	ddr3_1_dqs_n[2]	J26	Differential 1.35-V SSTL	Data strobe N byte 2
29	ddr3_1_dqs_p[3]	L23	Differential 1.35-V SSTL	Data strobe P byte 3
27	ddr3_1_dqs_n[3]	K22	Differential 1.35-V SSTL	Data strobe N byte 3
154	ddr3_1_dqs_p[4]	B26	Differential 1.35-V SSTL	Data strobe P byte 4
152	ddr3_1_dqs_n[4]	C27	Differential 1.35-V SSTL	Data strobe N byte 4
47	ddr3_1_dqs_p[5]	D18	Differential 1.35-V SSTL	Data strobe P byte 5

45	ddr3_1_dqs_n[5]	E19	Differential 1.35-V SSTL	Data strobe N byte 5
64	ddr3_1_dqs_p[6]	B23	Differential 1.35-V SSTL	Data strobe P byte 6
62	ddr3_1_dqs_n[6]	A23	Differential 1.35-V SSTL	Data strobe N byte 6
137	ddr3_1_dqs_p[7]	E25	Differential 1.35-V SSTL	Data strobe P byte 7
135	ddr3_1_dqs_n[7]	D25	Differential 1.35-V SSTL	Data strobe N byte 7
202	sodimm_scl	AC24	3.3-V LVTTTL	Clock connection for SODIMM
200	sodimm_sda	AD24	3.3-V LVTTTL	Data connection for SODIMM

Table 7: SODIMM pin assignments, signal name and functions

4.11 QSFP and SFP+ modules

The Komodo Fiber has 4 small form-factor pluggable (SFP) connector and cage assembly that accept SFP+ modules and one QSFP connector and cage assembly that accept QSFP module. Each SFP+ module can transmit\receive data at rates of up to 10Gb and the QSFP module can transmit\receive data at rates of up to 40Gb.

Board reference (JP1)	Signal Name	Arria V GZ Pin Number	I/O Standard	Description	
27	qsfp_modprsl	N24	3.3-V LVTTTL	Module present active low	
28	qsfp_intl	N23	3.3-V LVTTTL	Interrupt from QSFP active low	
11	qsfp_scl	AD6	2.5V	Serial I2C clock line	
12	qsfp_sda	AF6	2.5V	Serial I2C data line	
31	lpmode	-	-	Low power, pulled up to 3.3V	
9	qsfp_resetl	AG6	2.5V	Reset active low	
36	qsfp_txd[0]	AB4	1.5V PCML	Tx Data, each signal in differential with positive and negative connections	
37		AB3			
3	qsfp_txd[1]	AD4	1.5V PCML		
2		AD3			
33	qsfp_txd[2]	AF4	1.5V PCML		
34		AF3			
6	qsfp_txd[3]	AK4	1.5V PCML		
5		AK3			
17	qsfp_rxd[0]	AC2	1.5V PCML		Rx Data, each signal in differential with positive and negative connections
18		AC1			
22	qsfp_rxd[1]	AE2	1.5V PCML		
21		AE1			
14	qsfp_rxd[2]	AG2	1.5V PCML		
15		AG1			
25	qsfp_rxd[3]	AL2	1.5V PCML		
24		AL1			

Table 8: QSFP pin assignments, signal name and functions

Board reference	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
SFP+ module 1 (OP1)				
2	sfp_txflt[3]	AM23	3.3-V LVTTTL	Transmitter Fault Indication
8	sfp_lo[3]	R26	3.3-V LVTTTL	Loss of Signal
5	sfp_scl[3]	AK11	2.5 V	Serial I2C clock line
4	sfp_sda[3]	W10	2.5 V	Serial I2C data line
6	sfp_presn[3]	AP25	3.3-V LVTTTL	Reset, active low
3	sfp_tx_dis[3]	AD8	2.5 V	Transmitter Disable
7	sfp_rs_rx[3]	AP6	2.5 V	Received Data rate select, low selects reduced bandwidth
9	sfp_rs_tx[3]	AL8	2.5 V	Transmit Data rate select, low selects reduced bandwidth
13	sfp_rxd[3]	L2	1.5V PCML	Received Data Out, positive
12		L1	1.5V PCML	Received Data Out, negative
18	sfp_txd[3]	K4	1.5V PCML	Transmit Data In, positive
19		K3	1.5V PCML	Transmit Data In, negative
SFP+ module 2 (OP2)				
2	sfp_txflt[2]	AL23	3.3-V LVTTTL	Transmitter Fault Indication
8	sfp_lo[2]	T25	3.3-V LVTTTL	Loss of Signal
5	sfp_scl[2]	AK10	2.5 V	Serial I2C clock line
4	sfp_sda[2]	W9	2.5 V	Serial I2C data line
6	sfp_presn[2]	AN25	3.3-V LVTTTL	Reset, active low
3	sfp_tx_dis[2]	AD7	2.5 V	Transmitter Disable
7	sfp_rs_rx[2]	AN6	2.5 V	Received Data rate select, low selects reduced bandwidth
9	sfp_rs_tx[2]	AK8	2.5 V	Transmit Data rate select, low selects reduced bandwidth
13	sfp_rxd[2]	N2	1.5V PCML	Received Data Out, positive
12		N1	1.5V PCML	Received Data Out, negative
18	sfp_txd[2]	M4	1.5V PCML	Transmit Data In, positive
19		M3	1.5V PCML	Transmit Data In, negative
SFP+ module 3 (OP3)				
2	sfp_txflt[1]	AK23	3.3-V LVTTTL	Transmitter Fault Indication
8	sfp_lo[1]	T23	3.3-V LVTTTL	Loss of Signal
5	sfp_scl[1]	AK9	2.5 V	Serial I2C clock line
4	sfp_sda[1]	V10	2.5 V	Serial I2C data line
6	sfp_presn[1]	AP24	3.3-V LVTTTL	Reset, active low
3	sfp_tx_dis[1]	AG7	2.5 V	Transmitter Disable
7	sfp_rs_rx[1]	AM5	2.5 V	Received Data rate select, low selects reduced bandwidth
9	sfp_rs_tx[1]	AP7	2.5 V	Transmit Data rate select, low selects reduced bandwidth
13	sfp_rxd[1]	R2	1.5V PCML	Received Data Out, positive
12		R1	1.5V PCML	Received Data Out, negative

18	sfp_txd[1]	P4	1.5V PCML	Transmit Data In, positive
19		P3	1.5V PCML	Transmit Data In, negative
SFP+ module 4 (OP4)				
2	sfp_txflt[0]	AJ23	3.3-V LVTTTL	Transmitter Fault Indication
8	sfp_los[0]	R24	3.3-V LVTTTL	Loss of Signal
5	sfp_scl[0]	AJ9	2.5 V	Serial I2C clock line
4	sfp_sda[0]	U9	2.5 V	Serial I2C data line
6	sfp_presn[0]	AN24	3.3-V LVTTTL	Reset, active low
3	sfp_tx_dis[0]	AF7	2.5 V	Transmitter Disable
7	sfp_rs_rx[0]	AC11	2.5 V	Received Data rate select, low selects reduced bandwidth
9	sfp_rs_tx[0]	AN7	2.5 V	Transmit Data rate select, low selects reduced bandwidth
13	sfp_rxd[0]	W2	1.5V PCML	Received Data Out, positive
12		W1	1.5V PCML	Received Data Out, negative
18	sfp_txd[0]	V4	1.5V PCML	Transmit Data In, positive
19		V3	1.5V PCML	Transmit Data In, negative

Table 9: SFP+ pin assignments, signal name and functions

Near each SFP+ or QSFP module there are dual-color LEDs:

- 4 QSFP, dual color (green and yellow), active low LEDs
- 4 SFP+, dual color (green and yellow), active low LEDs

Board reference	Signal Name	Arria V GZ Pin Number	I/O Standard	Description	
D11	sfp_led_green[3]	AH10	2.5 V (Open drain)	User-defined LEDs (intended for showing transmit or receive activity on the SFP+ module). Driving logic 0 on the I/O port turns the LED on; driving high-z on the I/O turns the LED off	
	sfp_led_yellow[3]	AH9	2.5 V (Open drain)		
D12	sfp_led_green[2]	AG10	2.5 V (Open drain)		
	sfp_led_yellow[2]	AG9	2.5 V (Open drain)		
D13	sfp_led_green[1]	AF10	2.5 V (Open drain)		
	sfp_led_yellow[1]	AB9	2.5 V (Open drain)		
D14	sfp_led_green[0]	AF9	2.5 V (Open drain)		
	sfp_led_yellow[0]	AA9	2.5 V (Open drain)		
D15	qsfp_led_green[3]	AF8	2.5 V (Open drain)		User-defined LEDs (intended for showing transmit or receive activity on the QSFP module). Driving logic 0 on the I/O port turns the LED on; driving high-z on the I/O turns the LED off
	qsfp_led_yellow[3]	AD9	2.5 V (Open drain)		
D16	qsfp_led_green[2]	AE8	2.5 V (Open drain)		
	qsfp_led_yellow[2]	AC9	2.5 V (Open drain)		
D17	qsfp_led_green[1]	AJ8	2.5 V (Open drain)		
	qsfp_led_yellow[1]	AA8	2.5 V (Open drain)		
D18	qsfp_led_green[0]	AH8	2.5 V (Open drain)		
	qsfp_led_yellow[0]	Y9	2.5 V (Open drain)		

Table 10: SFP+ and QSFP LEDs pin assignments, signal name and functions

4.12 Fan Control (J6)

The fan that is connected to the heat-sink above the FPGA can be controlled with a dedicated I/O, as described in the following table:

Board reference (J6)	Signal Name	Arria V GZ Pin Number	I/O Standard	Description
1	fan_ctrl	AG24	3.3-V LVTTL	User controlled fan output. Driving logic 1 on the I/O port turns the FAN on; driving logic 0 on the I/O turns the FAN off

Table 11: Fan pin assignments, signal name and functions

5.1 Mechanical dimensions

The Komodo Fiber is a half-length, full-height, PCIe card according to PCI Express Card Electromechanical Specification, 111.16mm x 167.65mm.

The exact board mechanical dimensions are as defined in Figure 11.

For more detailed information please, contact KAYA Instruments representative.

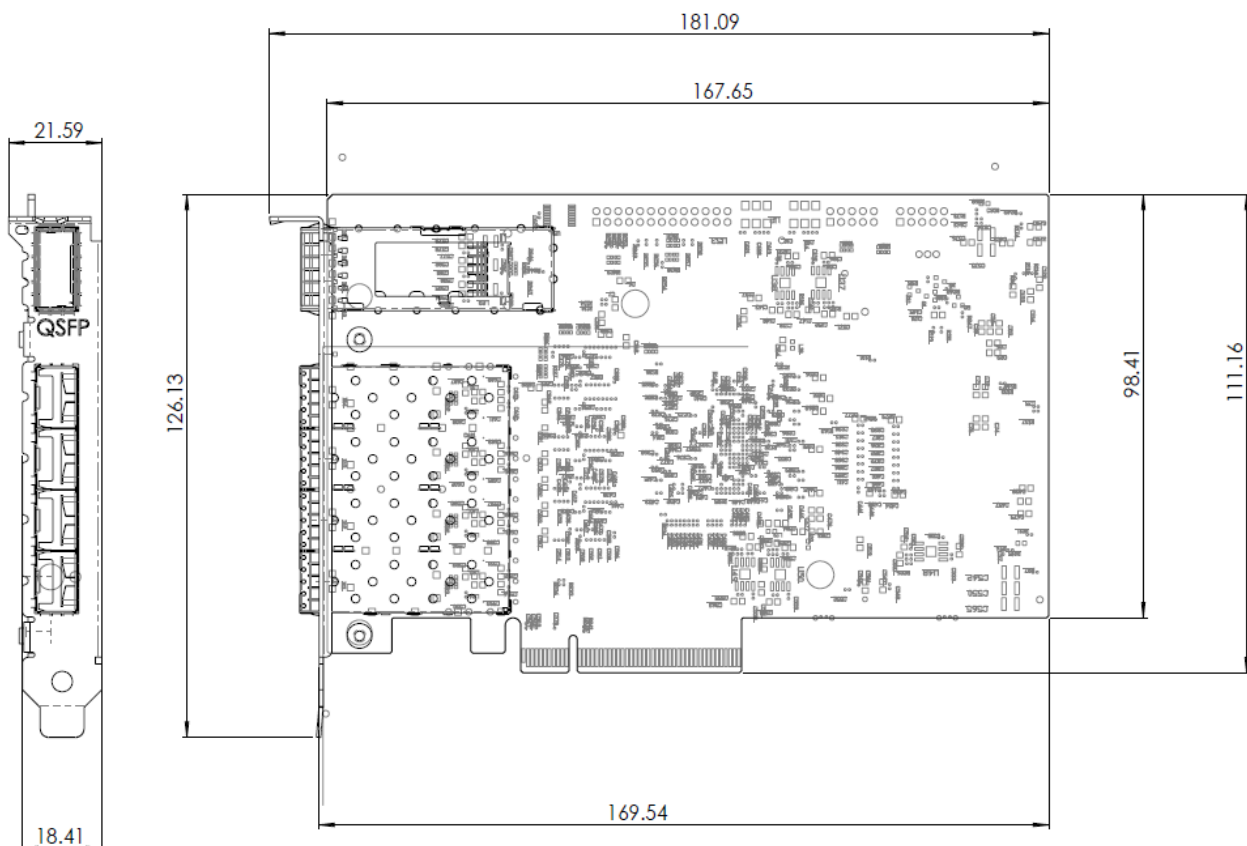


Figure 11: PCB Mechanical Dimensions

5.2 Absolute maximum ratings

Specification	Values
3.3V power supply	-1.0V to +7.0V
12V power supply	-0.3V to 14V
Storage temperature	-55°C to 125°C
Operating ambient temperature	0°C to 50°C

Table 12: Absolute maximum ratings

6.1 Power Supply

The Komodo Fiber is powered from the PCI Express edge connector. The input voltages must be in the range of $\pm 8\%$ of the nominal voltage. The DC voltage is stepped down to various power rails by the board components. Please pay careful attention not to draw more than the maximum Wattage from the power sources, as stated in the following table (see PCIe gen 3.0 specifications for more information):

Power Source	Voltage [V]	Current [A]	Maximum Wattage[W]
25-W PCI Express edge connector (when connected to PCIe gen 2.0 slot)	3.3	3.0	9
	12.0	2.1	16
75-W PCI Express edge connector (when connected to PCIe gen 3.0 slot)	3.3	3.0	9
	12.0	5.5	66

Table 13: Power input

6.2 Maximum and minimum input voltages

The minimum and maximum input voltages that the Komodo Fiber can endure are based on PCIe standard and shown in the table below.

Power Source [V]	Minimum Voltage [V]	Maximum Voltage [V]
3.3	3.04	3.56
12	11.04	12.96

Table 14: Maximum and minimum input voltages from PCIe

6.3 Power rails

The Komodo Fiber converts the 12V and 3.3V inputs to several other voltages, as shown in the table below.

Power Rail Name		Input Voltage [V]	Maximum Current [A]
FPGA	Other Component		
-	VCC1, VCCTX, VCCR _X (QSFP) VCC _{_TX} , VCC _{_RX} (SFP+)	3.3	12
VCCPGM, VCCIO3A, VCCIO3B, VCCPD3AB, VCCA_GXBL0, VCCA_GXBL1, VCCA_GXBR0, VCCA_GXBR1	-	3.0	3
VCCIO7A, VCCIO7B, VCCPD3CD, VCCPD4, VCCPD7, VCCPD8, VCCA_FPLL, VCC_AUX	-	2.5	3
VCCPT, VCCPGM, VCCH_GXBL0, VCCH_GXBL1, VCCH_GXBR0, VCCH_GXBR1, VCCD_FPLL	-	1.5	0.8

VCCIO3C, VCCIO3D, VCCIO4C, VCCIO4D, VCCIO7C, VCCIO7D, VCCIO8A, VCCIO8C, VCCIO8D	VDD, VDDQ (DDR3 SDRAM) VCC (DDR3 SODIMM)	1.35	8
VCCR_GXBL0, VCCR_GXBL1, VCCR_GXBR0, VCCR_GXBR1, VCCT_GXBL0, VCCT_GXBL1, VCCT_GXBR0, VCCT_GXBR1	-	1.0	0.8
VCC, VCCHIP_L, VCCHSSI_L, VCCHSSI_R	-	0.85	20

Table 15: Power rails on the KOMODO fiber board

6.4 Electrical characteristics for board IO's:

Symbol	Parameter	Condition	Pin	MIN	Typ	MAX	Units	
$ V_{OD} $	Differential Output Voltage	$R_L = 100 \Omega$	D _{OUT-} D _{OUT+}	250	350	450	mV	
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States				1	35	mV	
V_{OS}	Offset Voltage			1.12 5	1.23	1.375	V	
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				1	25	mV	
I_{OS}	Output Short Circuit Current ⁽⁴⁾	ENABLED, D _{IN} = V _{DD} , D _{OUT+} = 0 V or D _{IN} = GND, D _{OUT-} = 0 V			-5.8	-9.0	mA	
I_{OSD}	Differential Output Short Circuit Current ⁽⁴⁾	ENABLED, $V_{OD} = 0 V$			-5.8	-9.0	mA	
I_{OFF}	Power-off Leakage	V _{OUT} = 0 V or 3.6 V V _{DD} = 0 V or Open			-20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0 V and EN = V _{DD} V _{OUT} = 0 V or V _{DD}			-10	±1	+10	µA

Table 16: LVDS Output DC specifications (Driver Outputs)

Symbol	Parameter	Condition	Pin	MIN	Typ	MAX	Units	
V_{TH}	Differential Input High Threshold	$V_{CM} = 1.2 V, 0.05 V, 2.35 V$	R _{IN+} R _{IN-}		-15	35	mV	
V_{TL}	Differential Input Low Threshold			-100	-15		mV	
V_{CMR}	Common-Mode Voltage Range	V _{ID} = 100 mV, V _{DD} = 3.3 V			0.05		3	V
I_{IN}	Input Current	V _{DD} = 3.6 V V _{IN} = 0 V or 2.8 V			-12	±4	+12	µA
		V _{DD} = 0 V V _{IN} = 0 V or 2.8 V or 3.6 V		-10	±1	+10	µA	

Table 17: LVDS Input DC specifications (Receiver Inputs)

Symbol	Parameter	Test condition ^(*)	MIN	MAX	Units
V _{IH}	Input High Voltage	V _{OUT} ≥ V _{OH (min)} or V _{OUT} ≤ V _{OL (max)}	2	V _{DD} +0.3	V
V _{IL}	Input Low Voltage		-0.3	0.8	V
I _{IN}	Input Current	V _{IN} = 0 V or V _{IN} = V _{DD}		±5	μA

(*)V_{DD} = 3.3V, unless specified otherwise

Table 18: LVTTL input specifications

Symbol	Parameter	Test condition ^(*)	MIN	MAX	Units
V _{OH}	Output High Voltage	V _{DD} = min, I _{OH} = -2 mA	2.4		V
V _{OL}	Output Low Voltage	V _{DD} = min, I _{OL} = 2 mA		0.4	V

(*)V_{DD} = 3.3V, unless specified otherwise

Table 19: LVTTL output specifications

Symbol	Parameter	Test condition ^(*)	MIN	MAX	Units
V _{IH}	Input High Voltage	V _{OUT} ≥ V _{OH (min)} or V _{OUT} ≤ V _{OL (max)}	2	5	V
V _{IL}	Input Low Voltage		-0.3	0.8	V
I _{IN}	Input Current	V _{IN} = 0 V or V _{IN} = V _{DD}		±5	μA

(*)V_{DD} = 5V, unless specified otherwise

Table 20: TTL input specifications

Symbol	Parameter	Test condition ^(*)	MIN	MAX	Units
V _{OH}	Output High Voltage	V _{DD} = min, I _{OH} = -2 mA	4		V
V _{OL}	Output Low Voltage	V _{DD} = min, I _{OL} = 2 mA		0.4	V

(*)V_{DD} = 5V, unless specified otherwise

Table 21: TTL output specifications

The top level example design contains all the required project settings and an empty top level design for KOMODO Fiber in Verilog and VHDL.

The top level design files can be found under `fpga_top_level` folder in software CD.

The reference design demonstrates the basic operation of all the board interfaces. The reference design is supplied in open source Verilog code. The reference design is located under `fpga_reference_design` folder in the software CD. The following interfaces are included:

1. Onboard DDR3 Memory
2. SODIMM DDR3 Memory.
3. PCI Express
4. QSFP
5. SFP

8.1 Functional block diagram

Figure 12 shows the function diagram of the reference design.

The reference design includes a DDR3 controllers configured at 533 MHz with Quarter rate Avalon interface each for onboard DDR3 bank and an SODIMM bank. The controller for the SODIMM bank is configured to use MT8KTF51264HZ-1G6E1 SODIMM module from Micron. In addition to DDR3 memories the reference design includes PCI Express hard IP controller configured in Gen2 x8 lanes mode and a 10 gigabit Ethernet PHY connected to SFP+ and QSFP+ modules. A Signal TAP Logic analyzer and In System Sources and Probes IP are also connected in the design for control and monitoring.

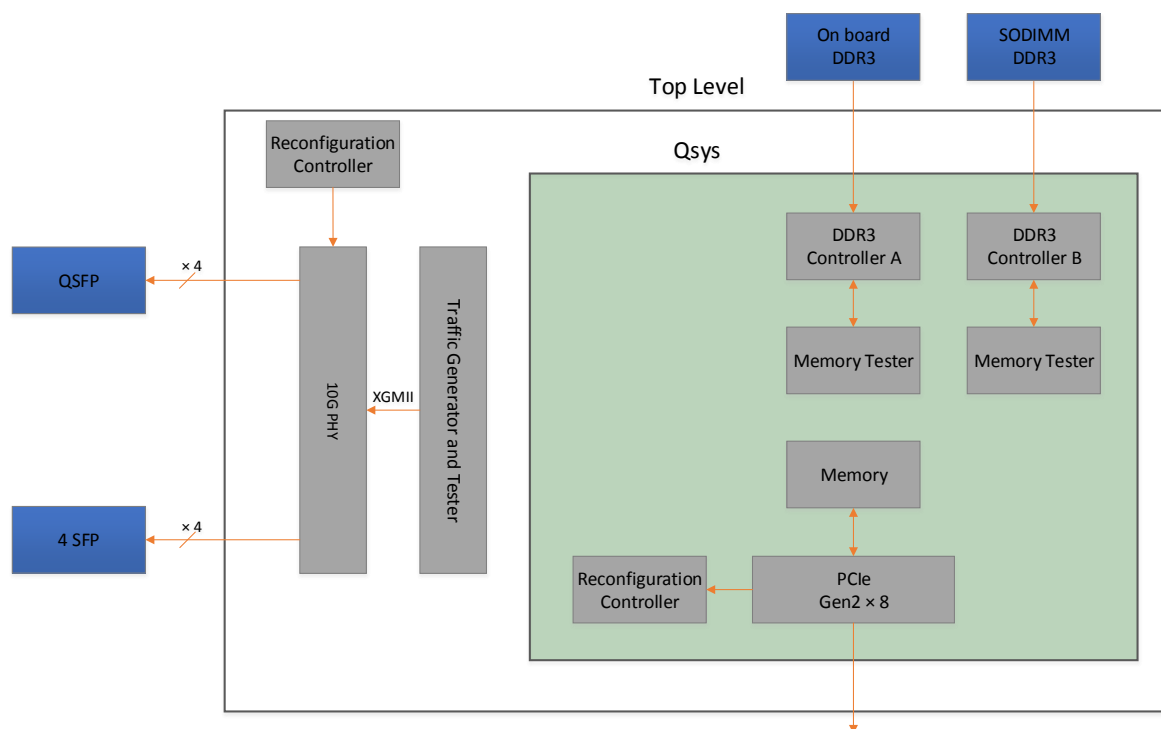


Figure 12: Function diagram

8.1.1 DDR3 memories

The reference design uses two DDR3 controllers from Altera to interface the onboard DDR3 bank and the SODIMM bank. For the SODIMM bank, the controller is configured to work with MT8KTF51264HZ-1G6E1 SODIMM from Micron.

Both the controllers are configured in Quarter rate (512bit) Avalon interface and operate at 533 MHz clock rate. The onboard DDR3 controller is configured as OCT (On Chip Termination) sharing master, while the SODIMM controller as slave.

The DDR3 controllers are driven by Altera Avalon-MM Traffic Generator IPs that performs a memory test after board reset.

The status of the memory test can be seen on board LEDs D3 and D4 for Onboard and SODIMM banks respectively. If the LED is lit the test have passed. The test status signals are also pulled to Signal TAP and In System Sources and Probes IP.

For more information about the DDR3 controller and traffic generator please visit Altera documentation at <http://www.altera.com/literature/lit-external-memory-interface.jsp>.

8.1.2 PCI Express

The PCI Express incorporates Altera hard IP configured in Gen2 x8 lanes mode. The IP is connected to internal FPGA SRAM. The SRAM can be read and written from the PC.

The PCI Express status signals are pulled to Signal TAP DS1 LED indicates that the PCI Express IP have entered L0 state.

For more information about the PCI Express IP please see Altera documentation at http://www.altera.com/literature/ug/ug_a5gz_pcie_avmm.pdf.

The access to the PCIe from PC can be made using JINGO driver that should be downloaded separately from <http://www.jungo.com/st/products/windriver/>.

KAYA instruments also offers PCI Express Gen3 x8 IP, High performance Scatter Gather DMA IP and a Drivers for DMA and PCI Express both for Windows and Linux. For IP licensing options please contact KAYA Instruments representative.

8.1.3 Ethernet PHY

For QSFP+ and SFP+ demonstration, Altera 10GBase-R PHY is used. The PHY is configured to 8 ports and connected both to SFP+ and QSFP+ modules. The XGMII side of the PHY is connected to KAYA traffic generator and tester. The traffic generator is an open source IP that generates and

sends 10Gbit Ethernet packets and verifies the received packets. The IP have a counter for received and transmitted packets. In case the received and transmitted packet counters match the LED of the specific port will be Green. In case the counters mismatch, the LED will be Red.

The test status and control signals of the traffic generator and tester are pulled to Signal TAP and In System Sources and Probes IP.

For more information about Altera PHY please visit http://www.altera.com/literature/ug/xcvr_user_guide.pdf.

8.2 Using the reference design

The reference design was designed for Quartus 64-Bit 15.0. In case other Quartus version is used, some Altera IPS might be need to be updated.

To use the reference design, please follow the following steps:

1. Make sure Quartus II is installed on your PC.
2. Install KOMODO Fiber board into the PC.
3. Connect the USB Blaster cable (or USB-Blaster II cable) to the KOMODO Fiber board and host PC. Install the USB Blaster driver if necessary
4. Power on the PC
5. Using Quartus programmer, load the ky_komodo_fiber.sof to the board. The file is located under fpga_reference_design \output_files\ folder in the software CD
6. Open ky_komodo_fiber.stp file to view the status signals
7. Open ky_komodo_fiber.spf file to control the Ethernet traffic generator
8. The LEDs of the board should indicate the statuses as described in Table 22.

Led Indicator	Functionality
DS1	Blinking in case PCI Express receives valid clock
DS2	Lit when PCI Express IP is in L0 state
DS3	Lit when onboard DDR3 bank passed test.
DS4	Lit when SODIMM DDR3 bank passed test.
QSFP+SFP LEDs	Red when traffic test failed, otherwise Green.

Table 22: LEDs description

8.3 Board Diagnostic

The reference design can be used as a board diagnostic to verify the board interfaces. The external board interfaces are verified through an external loopback method. To populate the external loopbacks, specific fixtures are required. Some of the fixtures are proprietary to KAYA Instruments. Please contact KAYA Instruments representative for availability of the fixtures.

For SFP+ loopback, optical SFP+ loopback fixtures are required. Figure 13 shows the optical SFP+ loopback fixture.

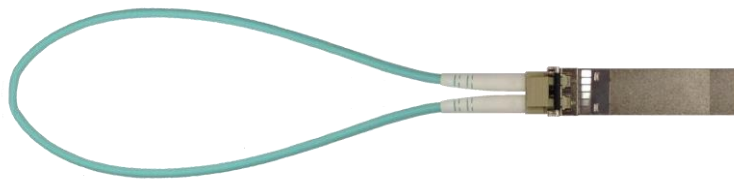


Figure 13: SFP+ loopback fixture

For QSFP loopback, optical QSFP loopback fixture is required. Figure 14 shows the optical QSFP loopback fixture.



Figure 14: QSFP loopback fixture

For DDR3 SODIMM test, a MT8KTF51264HZ-1G6E1 SODIMM from Micron is required as shown in Figure 15.



Figure 15: DDR3 SODIMM

The KOMODO Fiber board with all the loopback fixtures connected can be seen in Figure 16.

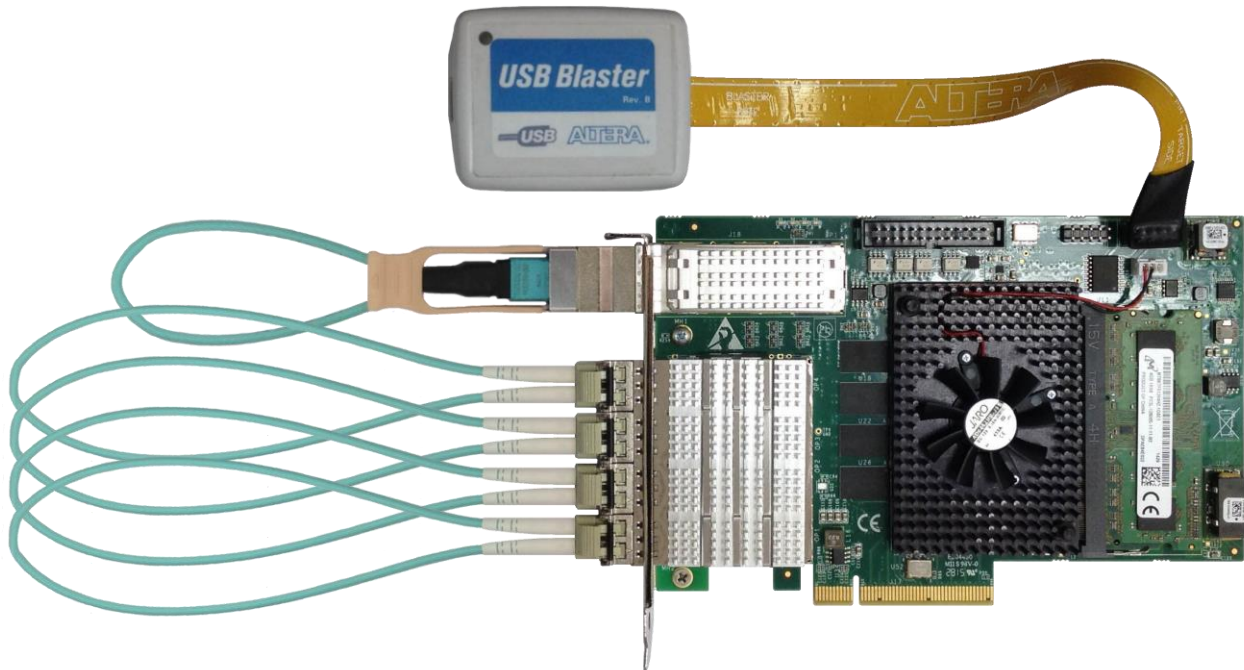


Figure 16: KOMODO Fiber with loopback fixtures

To run the diagnostic follow the below steps:

1. Make sure Quartus II is installed on your PC.
2. Install KOMODO Fiber board into the PC.
3. Connect the USB Blaster cable (or USB-Blaster II cable) to the KOMODO Fiber board and host PC. Install the USB Blaster driver if necessary
4. Connect the QSFP and SFP+ loopback fixtures to the board.
5. Power on the PC
6. Run diagnostic.bat file located under fpga_reference_design\output_files\ folder in the software CD.

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