4SXM (4S-XMC)

Altera Stratix® IV GX XMC with 4 SFP Transceivers

- High density Altera Stratix IV GX FPGA
- 4 SFP transceivers on front panel
- 8 multi-gigabit serial transceivers
- On-board oscillators for Fibre Channel, PCI Express, and Serial RapidIO
- 44 general purpose digital I/O

Based on Altera's Stratix IV GX FPGA, BittWare's 4S-XMC (4SXM) is a single-width XMC, designed to provide powerful FPGA processing and high-speed serial I/O capabilities to VME, VXS, VPX, cPCI, AdvancedTCA, or PCI Express carrier boards. The 4SXM features a high-density, low-power Altera Stratix IV GX FPGA, which was designed specifically for serial I/O-based applications and is PCI SIG compliant for PCI Express Gen1 and Gen2. Four small form-factor pluggable (SFP) compact optical transceivers are available on the front panel. Eight multi-gigabit serial lanes supporting PCI Express, Serial RapidIO, and 10 GigE are available via the board's rear panel as well as 44 general purpose digital I/O signals. The 4SXM also provides QDRII+ and Flash.

SFP Transceiver Interface

The 4SXM provides four SFP transceivers on the front panel with each transceiver providing support for virtually any serial communication standard, including: Fibre Channel, Gigabit Ethernet, SONET, CPRI, and OBSAI. The four SFP SerDes channels are connected directly to the Stratix IV GX FPGA. A 28-bit SFP control bus is also available to the Stratix IV GX.

Altera Stratix IV GX FPGA

The Altera Stratix IV GX was specifically designed for serial I/O-based applications requiring high-density, reconfigurable logic. The Stratix IV GX provides full-duplex, multi-gigabit transceivers, supporting PCI Express (Rev 1.0/2.0), 10 GigE, GigE, Serial RapidIO (Rev 1.0/2.0), and SerialLite II standards, as well as many others.

Rear Panel I/O

The 4SXM is compatible with BittWare's GTV6 or any other standard VME, VXS, VPX, CompactPCI, AdvancedTCA, or PCI Express carrier board equipped with an XMC interface. The board complies with the VITA 42.0 XMC standard, the VITA 42.2 Serial RapidIO standard, and the VITA 42.3 XMC PCI Express Protocol standard. The primary XMC connector (J15) provides 8 SerDes lanes directly to the Stratix IV GX, while XMC J14 provides 44 general-purpose digital I/O signals to the FPGA.

On-Board Oscillators

Three reference oscillators are available on the 4SXM. The standard set includes 106.25 MHz for Fibre Channel, 100 MHz for PCI Express, and 156.25 MHz for Serial RapidIO or 10 GigE.

Specifications

Board Architecture

FPGA

- Altera® Stratix® IV GX FPGA (4SGX110/180/230/290/360)

External Memory

- Up to 9 MBytes QDRII or QDRII+ SRAM configured as x18
- 128 MBytes of Flash memory for booting FPGA
- EEPROM for non-volatile ID and data storage

XMC Interface Connections

- 8 lanes SerDes which can support: 1-8x PCIe, two 4x Serial RapidIO, two 10 GigE, or any other serial protocol*
- 44 general-purpose digital I/O signals to Stratix IV GX via XMC J14

SFP Transceivers

- 4 SFP transceivers on front panel connected to Stratix IV GX via SerDes
- 28-bit SFP control bus connected to Stratix IV GX

On-Board Standard Reference Clocks

- 106.25 MHz oscillator for Fibre Channel
- 100 MHz oscillator for PCI Express
- 156.25 MHz oscillator for Serial RapidIO/10 GigE

JTAG Debug Interface

- On-board JTAG header or JTAG access via XMC J15 for Stratix IV GX debug

Mechanical

- Normal operational temperature: 0 to 50ºC
- Storage temperature: -20 to 70ºC
- Size: XMC single-width; 149 mm x 74 mm

Development Tools

FPGA Code Developement

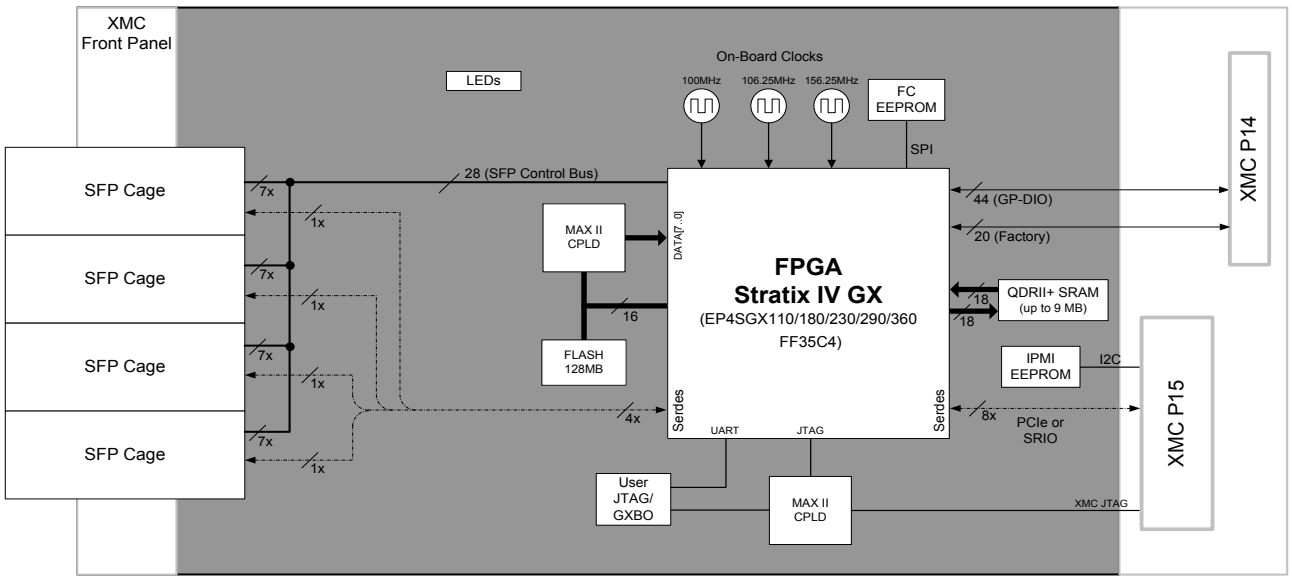
- Altera Quartus® II software

Accessory Boards

- BittWare XMBO for rear panel I/O breakout and debug
- BittWare GXBO breakout board for front panel I/O access

** SerDes max speed and protocol support may be FPGA speed grade dependent.*

Figure 3: 4SXM System Block Diagram



Ordering Options

4SXM-RW-AABB-CDE-FGHH-IJ					
RW	Ruggedization 0U = Commercial (0C to 50 C)*	AA	FPGA Size 11 = Altera Stratix IV GX 110* 18 = Altera Stratix IV GX 180 23 = Altera Stratix IV GX 230 29 = Altera Stratix IV GX 290 36 = Altera Stratix IV GX 360	BB	FPGA Temperature Range & Speed Grade C2 = Commercial / Speed Grade 2 C3 = Commercial / Speed Grade 3 C4 = Commercial / Speed Grade 4* I3 = Industrial / Speed Grade 3 I4 = Industrial / Speed Grade 4)
C	Flash Size 6 = 128 MB	D	QDRII/QDRII+ Size 0 = None 1 = 9 MB QDRII+ 2 = 9 MB QDRII *	E	Oscillator 0 = Standard (100, 106.25, 156.25 MHz)
F	SFP Cages 0 = None 4 = 4 cages	G	P12 Configuration 0 = Not populated 1 = Populated *	HH	SFP Transceivers 00 = No transceivers
I	Factory Configuration B = Blank P = PCIe S = SRIO X = XAUI	J	Environmental Assembly 6 = RoHS 6/6*		

* Default

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