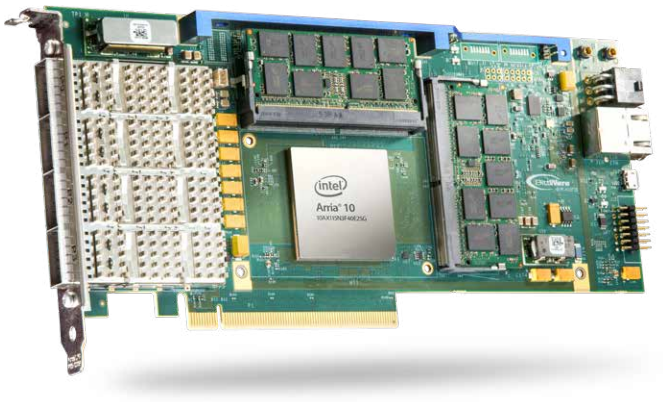
BittWare a molex company

Development Tools
Board Platforms
Integrated Platforms
Custom Solutions
Technology Partners

A10P3S

Arria® 10 GX/SX 3/4-Length PCIe Board with Quad QSFP and DDR4

- Intel Arria 10 GX/SX FPGA and SoC
- Up to two PCIe x8 interfaces supporting Gen1, Gen2, or Gen3
- Four QSFP cages for 4x 40GbE or 16x 10GbE
- Up to 40 GBytes of DDR4 SDRAM with ECC
- Board Management Controller for Intelligent Platform Management
- Timestamping support
- Utility I/O: 1000BASE-T Ethernet, USB 2.0, SATA



BittWare's A10P3S is a 3/4-length PCIe x8 card based on the Intel Arria 10 GX/SX FPGA and SoC. The Arria 10 boasts high densities and a power-efficient FPGA fabric married with a rich feature set including high-speed transceivers up to 28 Gbps, hard floating-point DSP blocks, and embedded Gen3 PCIe x8. The Arria 10 SX variant also features a dual-core ARM® Cortex™-A9 MPCore™ hard processor system (HPS). The board offers flexible memory configurations supporting over 40 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 40 Gbps. The A10P3S also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management. All of these features combine to make the A10P3S ideal for a wide range of applications, including network processing and security, compute and storage, instrumentation, broadcast, and SigInt.

Intel Arria 10 GX/SX FPGA and SoC

Built on 20 nm process technology, the Arria 10 FPGAs and SoCs feature industry-leading programmable logic that integrates a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers, and protocol IP controllers. The SX variant of the FPGA also incorporates a dual-core ARM® Cortex™-A9 MPCore™ hard processor system (HPS). Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Arria 10 to deliver floating point performance of up to 1.5 TFLOPS. The FPGA supports Gen3 PCIe x8 via hard IP blocks and provides up to 1150K equivalent LEs.

I/O Interfaces

The A10P3S provides a variety of interfaces for high-speed serial I/O as well as debug support. Four QSFP cages are available on the front panel, each supporting 40GbE or four 10GbE channels. The QSFP SerDes channels are connected directly to the Arria 10 FPGA, thus removing the latency of external PHYs. The QSFP cages can optionally be adapted for SFP+.

Two Gen3 x8 PCIe interfaces connect to the FPGA via 16 SerDes lanes, allowing for a x8 PCIe connection in a standard slot or two x8 interfaces in a bifurcated slot. Two SerDes lanes are available via SATA connectors to connect external storage devices or provide direct board-to-board communication. An Ethernet connector provides a 1000BASE-T connection to the SoC.

A USB 2.0 interface is available for debug and programming support. The USB features a built-in Intel USB-Blaster and is connected to the Board Management Controller. A USB-to-serial port is also available to the FPGA. The board supports timestamping with provision for a 1 PPS and reference clock input.

Memory

The A10P3S features two SODIMM sites that support up to 16 GBytes of DDR4 with optional error-correcting codes (ECC). Additional on-board memory includes up to 8 GBytes DDR4 and 64 MBytes flash for FPGA images. Boards with the Arria 10 SX also feature a MicroSD connector with a MicroSD memory card that includes the ARM/SoC operating system and filesystem.

Board Management Controller

Boards in BittWare's A10 family feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

Development Tools

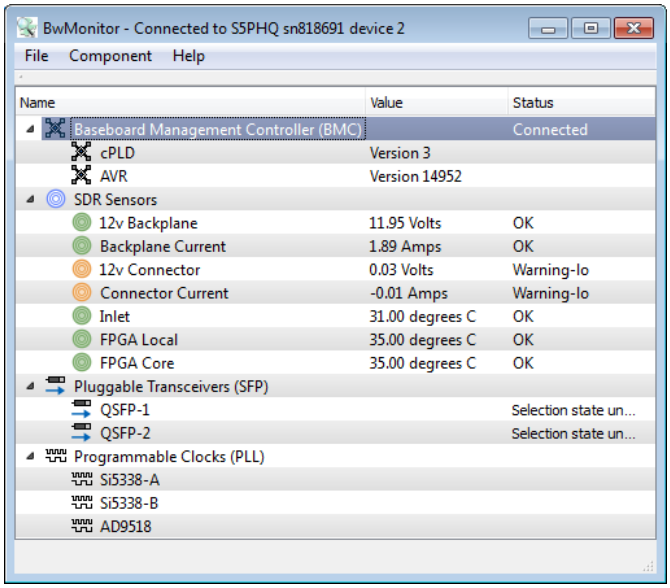
BittWorks II Toolkit

BittWare offers complete software support for the A10P3S with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Arria 10 FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

FPGA Development Kit

BittWare's FPGA DevKit provides FPGA board support IP and integration for BittWare's Intel FPGA-based boards. The FPGA DevKit includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR4, DDR3, DDR2, QDR2/+, PCIe, 10GbE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

BittWare Firmware and Network Solutions Partners

BittWare offers firmware for the Arria 10 FPGA on the A10 family PCIe boards, targeted specifically for networking applications. BittWare's FPGA framework provides a solid base for your application, including the following:

- 40GbE MAC
- 10GbE MAC
- PCIe multi-channel DMA engines
- DDR4 SDRAM, DDR3 SDRAM, and QDR-II controllers

BittWare has also partnered with several companies to offer solutions for networking and financial acceleration:

- Algo-Logic: Market feed handler and low latency gateway libraries, MAC, TOE
- Argon Design: Design services specializing in multimedia and FPGA-based high performance trading
- Atomic Rules: Custom IP development, example UDP, precision timestamping, PCIe, networking
- Enyx: UOE, TOE, book building IP, order management IP, Market Feed Handler
- Intilop: Ultra low latency TOE, UOE, and MAC
- LDA Technologies: 25 GbE Networking enclosures for PCI Express compliant FPGA board platforms
- LeWiz: Ultra low latency, multi-session TOE IP cores
- PolyBus: Infiniband link layer and transport layer
- Tamba Networks: Ultra low latency 10/40 GbE MAC + PCS, TOE

A10P3S
Specifications

Board Specifications

FPGA

- Intel® Arria® 10 GX/SX FPGA
- Dual-core ARM Cortex-A9 MPCore; up to 1.5 GHz CPU operation per core (SX only)
- High-performance, multi-gigabit SerDes transceivers @ 17 Gbps
- Up to 1150 (GX) or 660K (SX) logic elements available
- Up to 53 (GX) or 42 (SX) Mb of embedded memory
- 1.6 Gbps LVDS performance
- Up to 3,376 18x19 variable-precision multipliers

On-Board Memory

- One bank of up to 8 GBytes DDR4 (x32)
- 64 MBytes flash for FPGA images

MicroSD Card

- MicroSD card containing ARM/SoC OS and filesystem (SX only)

Optional SODIMM Memory

- DDR4: x72 w/ECC
  - Up to 16 GBytes per SODIMM

PCIe Interface

- Two x8 Gen1, Gen2, Gen3 interfaces direct to FPGA (One x8 interface in a standard slot; two x8 interfaces requires bifurcated slot)

USB Header

- Micro USB port (USB 2.0) for debug and programming FPGA and Flash
- Built-in Intel USB-Blaster
- FPGA serial port

Timestamp Support

- 1 PPS input
- Reference clock input

QSFP Cages

- 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 SerDes (no external PHY)
- Each supports 40GbE or 4x 10GbE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

Serial ATA

- Two SATA connectors, connected to FPGA

Ethernet

- RJ-45 Ethernet jack for 1000BASE-T connection to the SoC (SX only)

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- 3/4-length, standard-height PCIe slot card
- 241mm x 111.15mm
- Max. component height: 14.47mm

Development Tools

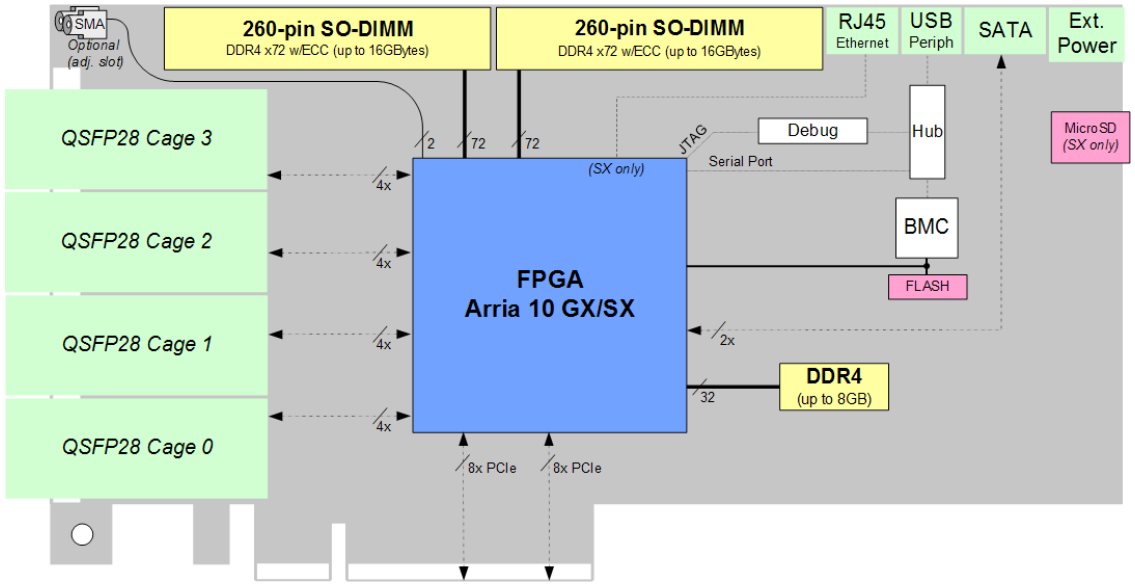
System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

FPGA HDL Development

- FPGA DevKit
  - Physical interface components
  - Board, I/O, and timing constraints
  - Example Quartus projects
  - Software components and drivers
- Intel Tools
  - Quartus II software, including Qsys
  - DSP Builder

Figure 2: A10P3S System Block Diagram



A10P3S Ordering Options

A10P3S-RW-ABBBBCDEF-GGHHII-JKLMN-OPQ-R

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)*
A	**A10 Printed Wiring Board** A = Optimized for 660 FPGA* B = Optimized for 1150 FPGA
BBBB	**Arria 10 Type and Size** 066S = Arria 10 SX 660 115X = Arria 10 GX 1150
C	**Arria 10 Transceiver Speed** 3 = 14.2 Gbps for GX* 4 = 12.5 Gbps for GX
D	**Arria 10 Temperature Range** E = 0C to 100C*
E	**Arria 10 Core Speed Grade** 1 = Faster 2 = Standard* 3 = Slower
F	**Arria 10 Power Options** L = Low static power S = Standard*
GG	**DDR4 Size and Configuration** 00 = None A4 = 2 GB (x32) B4 = 4 GB (x32)* C4 = 8 GB (x32)
HH	**SODIMM A** 0 0= None E3 = DDR4 8GB x72* E4 = DDR4 16GB x72
II	**SODIMM B** 0 0= None E3 = DDR4 8GB x72* E4 = DDR4 16GB x72
J	**QSFP Configuration** 4 = 4 QSFPs*
K	**Timing** X = On-board circuits only* S = Front panel SMAs (in next slot)
L	**JTAG** 0 = Embedded USB-Blaster 1 = Embedded USB-Blaster + Factory JTAG
M	**Oscillator** A = Adjustable TCXO† T = TCXO*
N	**Oscillator Configuration** 2 = None
O	**Heatsink** G = FPGA fansink, single-slot* H = FPGA heatsink, single-slot
P	**Misc. Configuration** 0 = Default
Q	**Mechanical Options** 6 = No stiffener S = Standard stiffener*
R	**Assembly** 6 = RoHS 6/6

* Default
† Contact Sky Blue or Zerif for availability

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