BittWare
a molex company

Development Tools
Board Platforms
Integrated Platforms
Technology Partners
Custom Solutions

A10PED

Dual Arria® 10 GX Full-Length PCIe Board
with Dual 12x Avago Fiber Optic, QSFP, and HMC

- Two Intel Arria 10 GX FPGAs
- Two PCIe x8 interfaces supporting Gen1, Gen2, or Gen3
- Two 12x Avago fiber optic modules
- QSFP cage for 4x 10GigE
- Memory options:
  - up to 2 GB Hybrid Memory Cube
  - up to 32 GBytes of DDR4 SDRAM with ECC
- Board Management Controller for Intelligent Platform Management
- Utility I/O: USB 2.0, SATA, powered GPIO header

BittWare's A10PED is a full-length PCIe x8 card featuring two Intel Arria 10 GX FPGAs. The Arria 10 boasts high densities and a power-efficient FPGA fabric married with a rich feature set including high-speed transceivers up to 15 Gbps, hard floating-point DSP blocks, and embedded Gen3 PCIe x8. The board offers flexible memory configurations, supporting a Hybrid Memory Cube along with up to 32 GBytes of memory. Two 12x Avago fiber optic modules and a QSFP cage provide high-speed, low-latency I/O direct to the FPGAs. The A10PED also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management. All of these features combine to make the A10PED ideal for a wide range of applications, including network processing and security, compute and storage, instrumentation, broadcast, and SigInt.

Intel Arria 10 GX FPGA

Built on 20 nm process technology, the Arria 10 FPGAs feature industry-leading programmable logic that integrates a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers, and protocol IP controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Arria 10 to deliver floating point performance of up to 1.5 TFLOPS. The FPGA supports Gen3 PCIe x8 via hard IP blocks and provides up to 1150K equivalent LEs.

I/O Interfaces

The A10PED provides a variety of interfaces for high-speed serial I/O as well as debug support. Two 12x Avago fiber optic modules are on the front panel, supporting high-density, high-speed optical interconnects. A QSFP cage is also available on the front panel, supporting four 10GigE channels. The Avago and QSFP SerDes channels are connected directly to the Arria 10 FPGAs, thus removing the latency of external PHYs. The QSFP cage can optionally be adapted for SFP+.

Several additional interfaces also support high-speed I/O. Two Gen3 x8 PCIe interfaces connect to the FPGAs via 16 SerDes lanes, allowing for a x8 PCIe connection (to FPGA A) in a standard slot or two x8 interfaces (one to each FPGA)in a bifurcated slot. Two SerDes lanes are available via SATA connectors to connect external storage devices or provide direct board-to-board communication.

A USB 2.0 interface provides debug and programming support. The USB features a built-in Intel USB-Blaster and is connected to the Board Management Controller. The board also provides an on-board powered GPIO header.

Memory

The A10PED features four SODIMM sites, each supporting up to 8 GBytes of DDR4 with optional error-correcting codes (ECC). A Hybrid Memory Cube (HMC) provides high-performance serial memory. Additional on-board memory includes flash with factory default and support for multiple FPGA images.

Board Management Controller

Boards in BittWare's A10 family feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

Development Tools

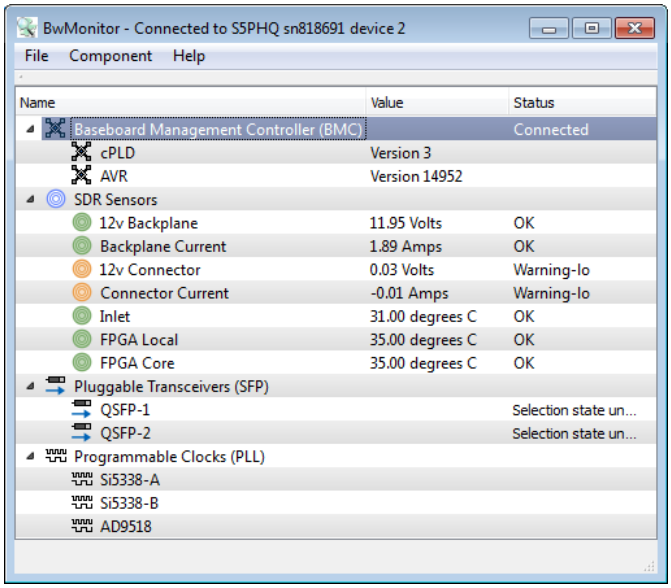
BittWorks II Toolkit

BittWare offers complete software support for the A10PED with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Arria 10 FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

FPGA Development Kit

BittWare's FPGA Development Kit provides FPGA board support IP and integration for BittWare's Intel FPGA-based boards. The FPGA DevKit includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR4, PCIe, 10GigE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

BittWare Firmware and Network Solutions Partners

BittWare offers firmware for the Arria 10 FPGA on the A10 family PCIe boards, targeted specifically for networking applications. BittWare's FPGA framework provides a solid base for your application, including the following:

- 10GigE MAC
- PCIe multi-channel DMA engines
- DDR4 SDRAM controllers

BittWare has also partnered with several companies to offer solutions for networking and financial acceleration:

- Algo-Logic: Market feed handler and low latency gateway libraries, MAC, TOE
- Argon Design: Design services specializing in multimedia and FPGA-based high performance trading
- Atomic Rules: Custom IP development, example UDP, precision timestamping, PCIe, networking
- Enyx: UOE, TOE, book building IP, order management IP, Market Feed Handler
- Intilop: Ultra low latency TOE, UOE, and MAC
- LDA Technologies: 25 GbE Networking enclosures for PCI Express compliant FPGA board platforms
- LeWiz: Ultra low latency, multi-session TOE IP cores
- PolyBus: Infiniband link layer and transport layer
- Tamba Networks: Ultra low latency 10/40/100 GigE MAC + PCS, TOE

A10PED
Specifications

Board Specifications

FPGA

- Intel® Arria® 10 GX FPGA
- High-performance, multi-gigabit SerDes transceivers @ up to 17 Gbps
- Up to 1150 logic elements available
- Up to 53 Mb of embedded memory
- 1.6 Gbps LVDS performance
- Up to 3,376 18x19 variable-precision multipliers

On-Board Memory

- Flash memory for booting FPGA

Hybrid Memory Cube (HMC)

- Up to 2 GByte Hybrid Memory Cube connected to each FPGA via 16x SerDes

Optional SODIMM Memory

2 per FPGA; can be any of the following:

- DDR4: x72 w/ECC
  - Up to 8 GBytes per SODIMM

PCIe Interface

- Two x8 Gen1, Gen2, Gen3 interfaces direct to FPGAs: one x8 interface (to FPGA A) in a standard slot; two x8 interfaces (one to each FPGA) requires bifurcated slot

USB Header

- Micro USB port (USB 2.0) for debug and programming FPGA and Flash
- Built-in Intel USB-Blaster

Avago Fiber Optic

- Two 12x Avago fiber optic modules, connected to the FPGAs via 12 SerDes channels each

QSFP Cages

- QSFP28 (zQSFP) cage on front panel connected directly to each FPGA via 2 SerDes (no external PHY)
- Supports 4x 10GigE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

Serial ATA

- Two SATA connectors, connected to FPGAs

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- Full-length, standard-height, double-wide PCIe slot card

Development Tools

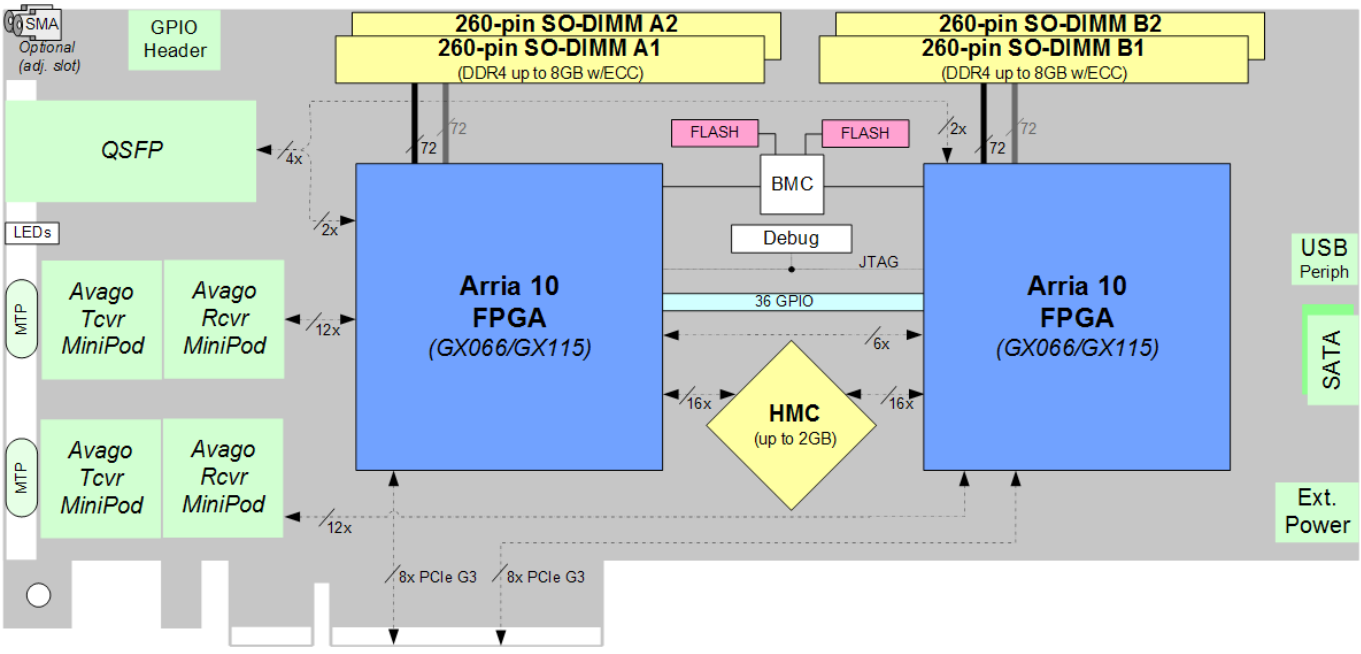
System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

FPGA HDL Development

- FPGA Development Kit
  - Physical interface components
  - Board, I/O, and timing constraints
  - Example Quartus projects
  - Software components and drivers
- Intel Tools
  - Quartus II software, including Qsys
  - DSP Builder

Figure 2: A10PED System Block Diagram



A10PED Ordering Options

A10PED-RW-A-BBBBCDEF-G-HHII-J-KKKKLMNO-P-QQRR-O-O-UVWXYZ-AB

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)*
A	**A10 Printed Wiring Board** A = Optimized for 660 FPGA* B = Optimized for 1150 FPGA †
BBBB	**Arria 10 A Type and Size** 066X = Arria 10 GX 660* 115X = Arria 10 GX 1150 †
C	**Arria 10 A Transceiver Speed** 0 = None 3 = 14.2 Gbps for GX* 4 = 12.5 Gbps for GX
D	**Arria 10 A Temperature Range** E = 0C to 100C*
E	**Arria 10 A Core Speed Grade** 1 = Faster 2 = Standard* 3 = Slower
F	**Arria 10 A Power Options** L = Low static power S = Standard*
G	**FPGA A Front Panel Optics** N = Empty sockets* I = Rx module, empty Tx socket O = Tx module, empty Rx socket B = Bi-directional
HH	**FPGA A SODIMM A** 0 0= None E2 = DDR4 4GB x72* E3 = DDR4 8GB x72
II	**FPGA A SODIMM B** 0 0= None E2 = DDR4 4GB x72* E3 = DDR4 8GB x72
J	**HMC** 0 = None 1 = 2GB*
KKKK	**Arria 10 B Type and Size** 066X = Arria 10 GX 660 115X = Arria 10 GX 1150
L	**Arria 10 B Transceiver Speed** 3 = 14.2 Gbps for GX* 4 = 12.5 Gbps for GX
M	**Arria 10 B Temperature Range** E = 0C to 100C*
N	**Arria 10 B Core Speed Grade** 1 = Faster 2 = Standard* 3 = Slower
O	**Arria 10 B Power Options** L = Low static power S = Standard*
P	**FPGA B Front Panel Optics** N = Empty sockets* I = Rx module, empty Tx socket O = Tx module, empty Rx socket B = Bi-directional
QQ	**FPGA B SODIMM A** 0 0= None E2 = DDR4 4GB x72* E3 = DDR4 8GB x72
RR	**FPGA B SODIMM B** 0 0= None E2 = DDR4 4GB x72* E3 = DDR4 8GB x72
U	**Timing** 0 = On-board circuits only S = Front panel SMAs*
V	**Oscillator** A = Adjustable TCXO† T = TCXO*
W	**Auxilliary Oscillator** 2 = None*
X	**Heatsink - FPGA** A = Active* P = Passive
Y	**Heatsink - HMC** A = Active P = Passive*
AZ	**Mechanical Options** 0 = No stiffener S = Standard stiffener*
A	**Misc. Configuration** 0 = Default
B	**Assembly** 6 = RoHS 6/6

* Default.
† Contact Sky Blue and Zerif.

Contact

Sky Blue Microsystems GmbH
Geisenhausenerstr. 18
81379 Munich, Germany
+49 89 780 2970, info@skyblue.de
www.skyblue.de

In Great Britain:
Zerif Technologies Ltd.
H5 Ash Tree Court
Nottingham NG8 6PY, England
+44 115 855 7883, info@zerif.co.uk
www.zerif.co.uk