

## A10PL4

### Arria® 10 GX Low Profile PCIe Board with Dual QSFP and DDR4

- Intel Arria 10 GX FPGA
- PCIe x8 interface supporting Gen1, Gen2, or Gen3
- Dual QSFP cages for 2x 40GbE or 8x 10GbE
- Memory: up to 32 GBytes of DDR4 SDRAM with ECC (x72)
- Board Management Controller for Intelligent Platform Management
- Precision clock and timing options
- Utility I/O: USB 2.0



BittWare's A10PL4 is a low-profile PCIe x8 card based on the Intel Arria 10 GX FPGA. The Arria 10 boasts high densities and a power-efficient FPGA fabric married with a rich feature set including high-speed transceivers, hard floating-point DSP blocks, and embedded Gen3 PCIe x8. The board offers over 32 GB of memory, sophisticated clocking and timing options, and two front panel QSFP cages, each supporting . The A10PL4 also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management. All of these features combine to make the A10PL4 ideal for a wide range of applications, including network processing and security, compute and storage, instrumentation, broadcast, and SigInt.

#### Intel Arria 10 GX FPGA

Built on 20 nm process technology, the Arria 10 FPGAs feature industry-leading programmable logic that integrates a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers, and protocol IP controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Arria 10 to deliver floating-point performance of up to 1.5 TFLOPS. The FPGA supports Gen3 PCIe x8 via a hard IP block and provides up to 1150K equivalent LEs.

#### I/O Interfaces

The A10PL4 provides a variety of interfaces for high-speed serial I/O as well as debug support. Two QSFP cages are available on the front panel, each supporting 40GbE or four 10GbE channels. The QSFP SerDes channels are connected directly to the Arria 10 FPGA, thus removing the latency of external PHYs. The QSFP cages can optionally be adapted for SFP+.

The x8 PCIe interface provides 8 SerDes lanes to the Arria 10 FPGA. A USB 2.0 interface with built-in USB-Blaster is available for debug and programming support. The board also supports timestamping with an optional precision timing module, which features 1 PPS and reference clock inputs and outputs along with precision clock circuitry. The timing module option requires a full-height front panel.

#### Memory

The A10PL4 features up to 32 GBytes of DDR4 with optional error-correcting codes (ECC). Additional on-board memory includes flash memory with factory default and support for multiple FPGA images. An on-board PROM provides access to the board's MAC ID.

#### OpenCL™ Support

The A10PL4 supports the Open Computing Language (OpenCL™) programming model, providing an incredibly powerful solution for system acceleration. Development tools for OpenCL include Intel's SDK for OpenCL and BittWare's OpenCL Developer's Bundle.



# A10PL4

## Board Management Controller

Boards in BittWare's A10 family feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

## Development Tools

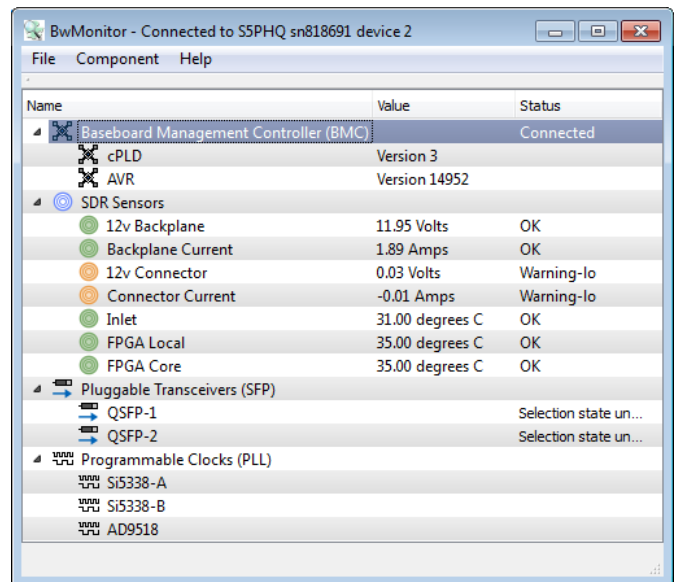
### BittWorks II Toolkit

BittWare offers complete software support for the A10PL4 with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Arria 10 FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

## FPGA Development Kit

BittWare's FPGA DevKit provides FPGA board support IP and integration for BittWare's Intel FPGA-based boards. The FDK includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR4, DDR3, DDR2, QDR2/+, PCIe, 10GbE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

## BittWare Firmware and Network Solutions Partners

BittWare offers firmware for the Arria 10 FPGA on the A10 family PCIe boards, targeted specifically for networking applications. BittWare's FPGA framework provides a solid base for your application, including the following:

- 10GbE MAC
- PCIe multi-channel DMA engines
- DDR4 SDRAM and QDR11/II+ controllers

BittWare has also partnered with several companies to offer solutions for networking and financial acceleration:

- **Algo-Logic:** Market feed handler and low latency gateway libraries, MAC, TOE
- **Argon Design:** Design services specializing in multimedia and FPGA-based high performance trading
- **Atomic Rules:** Custom IP development, example UDP, precision timestamping, PCIe, networking
- **Enyx:** UOE, TOE, book building IP, order management IP, Market Feed Handler
- **Intilop:** Ultra low latency TOE, UOE, and MAC
- **LDA Technologies:** 25 GbE Networking enclosures for PCI Express compliant FPGA board platforms
- **LeWiz:** Ultra low latency, multi-session TOE IP cores
- **PolyBus:** Infiniband link layer and transport layer
- **Tamba Networks:** Ultra low latency 10/40 GigE MAC + PCS, TOE

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### Specifications

#### BOARD SPECIFICATIONS

##### FPGA

- Intel® Arria® 10 GX FPGA
- High-performance, multi-gigabit SerDes transceivers @ up to 17 Gbps
- Up to 1150K logic elements available
- Up to 53 Mb of embedded memory
- 1.6 Gbps LVDS performance
- Up to 3,300 18x19 variable-precision multipliers

##### On-Board Memory

- Two banks DDR4 with ECC, up to 16 GBytes (x72) each
- 128 MBytes of Flash memory for booting FPGA

##### PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

##### USB Header

- USB 2.0 interface for debug and programming FPGA and Flash
- Built-in Intel USB-Blaster

#### Precision Timing Module(Optional)

- 1 PPS input and output
- Reference clock input and output
- Adjustable TCXO

#### QSFP Cages

- 2 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 8 SerDes (no external PHY)
- Each supports 40GbE or 4 10GbE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

#### Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I<sup>2</sup>C bus access
- USB 2.0 and JTAG access
- Voltage overrides

#### Size

- Low profile (Half-height, half-length) PCIe slot card; x8 mechanical
- 168mm x 68.9mm
- Max. component height: 14.47mm

#### DEVELOPMENT TOOLS

##### System Development

- [BittWorks II Toolkit](#) - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

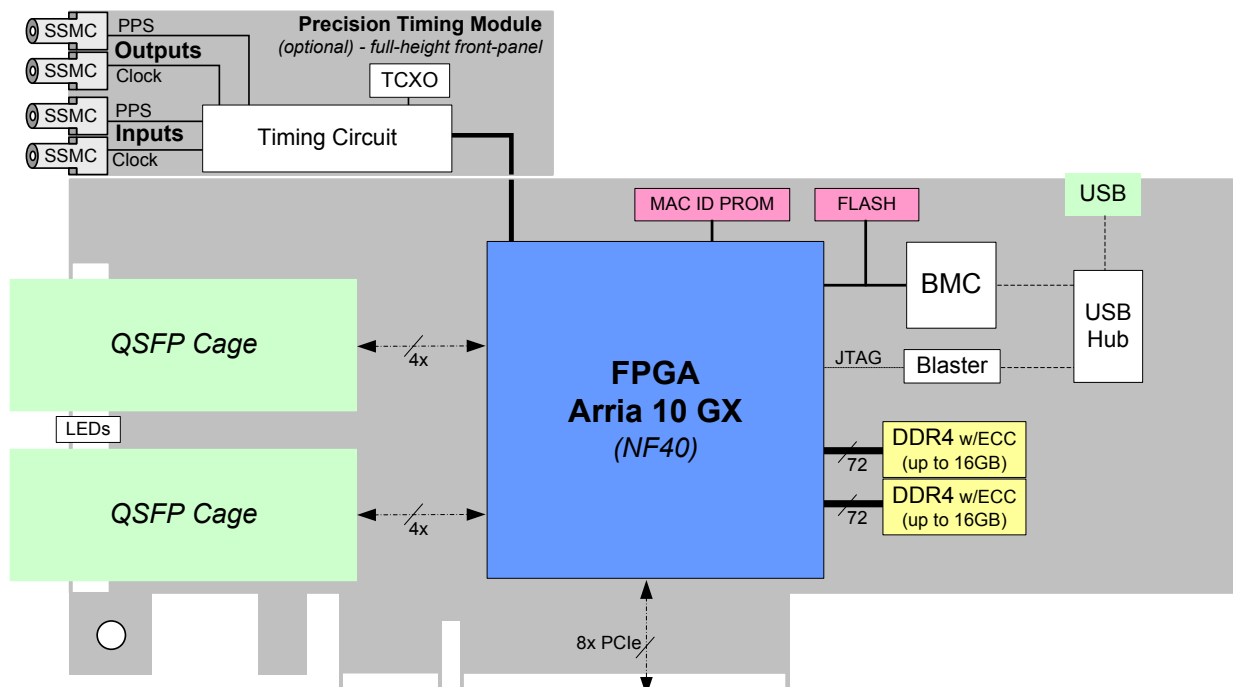
##### FPGA HDL Development

- [FPGA DevKit](#)
  - Physical interface components
  - Board, I/O, and timing constraints
  - Example Quartus projects
  - Software components and drivers
- [Intel Tools](#)
  - Quartus II software

##### OpenCL Development

- [OpenCL Developer's Bundle](#) - BittWorks II Toolkit, Board Support Packages, Intel SDK for OpenCL, Intel Quartus II

Figure 2: A10PL4 System Block Diagram

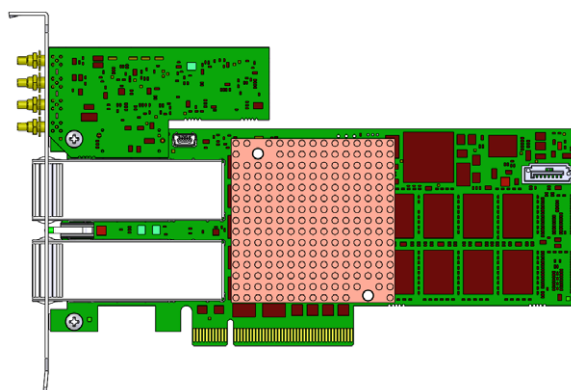


## A10PL4 Ordering Options

A10PL4-RW-ABBBBCDEF-GH-IJKLMN-O			
RW	Ruggedization 0U = Air cooled (0°C to 50°C)*	H	DDR4 Bank B 0 = None 2 = 4 GB* 3 = 8 GB 4 = 16 GB †
A	A10 Printed Wiring Board A = Optimized for 660 FPGA B = Optimized for 1150 FPGA*	I	Front Panel H = Half-height * F = Full-height T = Full-height with Precision Timing Module
BBBB	Arria 10 Type and Size 115X = Arria 10 GX 1150* 066X = Arria 10 GX 660	J	Flash Configuration 1 = Standard (HDL tool flow)* 2 = OpenCL
C	Arria 10 Transceiver Speed 3 = 14.2 Gbps for GX* 4 = 12.5 Gbps for GX	K	QSFP 0 = Not installed 1 = Installed*
D	Arria 10 Temperature Range E = 0C to 100C*	L	Heatsink P = Passive A = Active*
E	Arria 10 Core Speed Grade 1 = Faster 2 = Standard* 3 = Slower	M	Oscillator 0 = Standard*
F	Arria 10 Power Options L = Low static power S = Standard*	N	Miscellaneous 1 = Default
G	DDR4 Bank A 0 = None 2 = 4 GB* 3 = 8 GB 4 = 16 GB †	O	Assembly 6 = RoHS 6/6

\* Default

† Contact Sky Blue or Zerif for availability



A10PL4 with Precision Timing Module

DS-A10PL4 | Rev 2018.11.13 | November 2018

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