D4AM (D4-AMC)

Dual Altera Stratix® IV FPGA AdvancedMC with VITA 57 Site

- Dual FPGAs: Altera Stratix IV E and Stratix IV GX
- BittWare's FINe™ III Host/Control Bridge provides control plane processing and interface
- VITA 57 FMC site for I/O and processing expansion
- AMC I/O: 18 ports SerDes, 1 port GigE
- Additional I/O: 10/100 Ethernet, 16 GPIO, RS-232, and JTAG

BittWare's D4-AMC (D4AM) features the I/O processing power of two Altera Stratix IV FPGAs. The D4AM is a mid- or full-size, single wide AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. An Altera Stratix IV GX FPGA paired with a Stratix IV E make the D4AM an extremely high-density, flexible board. The FPGAs are connected by two full-duplex 2 GByte/sec lanes of parallel I/O for data sharing. Providing enhanced flexibility is a VITA 57-compliant FMC site, which connects directly to the Stratix IV E FPGA for LVDS and to the Stratix IV GX for SerDes.

The board also provides an IPMI system management interface and a configurable 18-port AMC SerDes interface supporting a variety of protocols. On-board memory includes up to 1 GByte of DDR3 and 128 MBytes of Flash, and Ethernet is available via the AMC front and rear panels.

Altera Stratix IV GX FPGA

The Altera Stratix IV GX FPGA was specifically designed for serial I/O-based applications requiring high-density, reconfigurable logic. The Stratix IV GX provides 18 full-duplex, multi-gigabit transceivers, 16 of which are high-performance supporting PCI Express (Rev 1.0/2.0), 10 GigE, GigE, Serial RapidIO (Rev 1.0/2.0), and SerialLite II standards. It contains up to 530k equivalent logic elements, over 20 Mbits of embedded memory, and 1,024 embedded 18x18 multipliers.

Altera Stratix IV E FPGA

The Altera Stratix IV E (Enhanced) is a high-density FPGA that provides up to 813,050 logic elements, over 33 Mbits of embedded memory, and 1,288 18x18 bit multipliers. The Stratix IV E is connected to the Stratix IV GX by a 184-bit, 250 MHz user I/O interface.

Fat Pipes, Common Options, and I/O Interfaces

The Stratix IV GX FPGA interfaces to 2 ports (1, 2) in the AMC common options region, and 16 ports (8 of which are optional) in the AMC fat pipes region (4 - 15, 17 - 20). These 18 ports provide a network data and control switch fabric interface on the AMC connector, with 16 supporting up to 6.25 GHz and 2 supporting up to 3.125 GHz. Port 0 provides a GigE interface. All AMC clocks are also connected to the Stratix IV GX.

Front panel I/O includes a debug utility header that provides access to 10/100 Ethernet, 2 RS-232 ports, and a JTAG port for debug support. An auxiliary I/O header on the front panel provides access to Stratix IV E FPGA I/O signals.

VITA 57 FMC Site for Processing and I/O Expansion

The D4AM features an FMC (FPGA Mezzanine Card) site, which provides 8 high-performance SerDes, 80 LVDS pairs, and 6 clocks connected to the Stratix IV. The site is based on the VITA 57 mezzanine standard for FPGA I/O, enabling designers to customize the D4AM to their individual needs with optional FMC I/O boards. A variety of I/O or processor FMCs are available integrated with the D4AM.

FINe™ III Host/Control Bridge

BittWare's FINe III Host/Control Bridge implements a complete control plane interface for the D4AM, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. Extensive software support is provided via BittWare's BittWorks Toolkit, which is tightly integrated with the FINe.

The FINe III provides GigE via the common options region, along with 10/100 Ethernet and an RS-232 monitor port via a debug utility header, and is connected to the FPGAs via a local control bus.

Development Tools

BittWare offers complete software support for the D4AM with its BittWorks II Toolkit. BittWorks II is a suite of software development tools, designed to make developing and debugging applications for BittWare's signal processing boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely. The BittWorks software tools include host interface libraries, a wide variety of diagnostic utilities and configuration tools, debug tools, and I/O drivers.

Data Conversion and Processor FMC Options

A variety of VITA-57 FMCs are available to add I/O or Anemone processors to the D4AM's VITA-57 FMC site:

- 3F104: 4 channels 14-bit, 250 MSPS ADC
- 3F107: 8 channels 12-bit, 65 MSPS ADC
- 3F125: 1-4 channels 8-bit, up to 5 GSPS ADC
- 3F126: 1-4 channels 10-bit, up to 5 GSPS ADC
- 3F150: 2 channels, 14-bit, 250 MSPS ADC and 2 channels, 16-bit, 800 MSPS DAC
- 3F204: 1 - 4 channels 16-bit, up to 1 GSPS DAC
- SPFM: 4 front-panel SFP transceivers
- AAFM: 4 Anemone104 co-processors

D4AM (D4-AMC)

Specifications

Board Architecture

Stratix IV GX FPGA

- Altera® Stratix® IV GX FPGA (4SGX180/230/290/360/530)
- 16 full-duplex, high-performance, multi-gigabit SerDes transceivers @ 6.25 GHz
- 2 full-duplex, multi-gigabit SerDes transceivers @ 3.125 GHz
- Over 530k equivalent LEs
- Over 20 Mbits of RAM
- Over 1,024 embedded multipliers

Stratix IV E FPGA

- Altera® Stratix® IV E FPGA (4SE360/530/820)
- Over 813k equivalent LEs
- Over 33 Mbits of RAM
- 1,288 18x18 embedded multipliers

BittWare FINe III Host/Control Bridge

- GigE to rear panel
- Supports host- and Flash-based booting of Stratix IV GX FPGA
- Runs BittWorks server for full remote access via the BittWare Toolkit

External Memory

- 4 banks of up to 256 MByte DDR3 SDRAM configured as x16 (2 per FPGA)
- 128 MBytes of Flash memory for booting FPGA and FINe

Fat Pipes Interface

- 16 (8 are optional) ports (4 - 11, 12-15, 20 - 17) @ up to 6.25 GHz, configurable to support PCI Express (Rev 1.0/2.0), Serial RapidIO (Rev 1.0/2.0), GigE, 10GigE/XAUI

Common Options Interface

- BittWare's FINe™ III Host/Control Bridge providing GigE on port 0
- Ports 1 & 2 configurable to support PCI Express, Serial RapidIO, and GigE

Other AMC Edge Connections

- All AMC clocks brought to FPGA
- Module Management Control (MMC) Interface implementing IPMI for temperature monitoring and hot-swap support

I/O Interfaces

- 10/100 Ethernet to FINe
- RS-232 port to Stratix IV GX
- RS-232 port to FINe
- JTAG debug interface to the Stratix IV GX
- 16 auxiliary I/O signals to Stratix IV E

VITA 57 FMC Site

- VITA 57-compliant
- Optional 8x high-performance SerDes to Stratix IV GX
- 80 LVDS pairs to Stratix IV E
- 6 clocks to FPGA

Size

- AMC mid-size or full-size, single width format compatible with AMC.0 specification R2.0

Development Tools

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks II Porting Kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems

FPGA Development

- Altera Quartus® II software

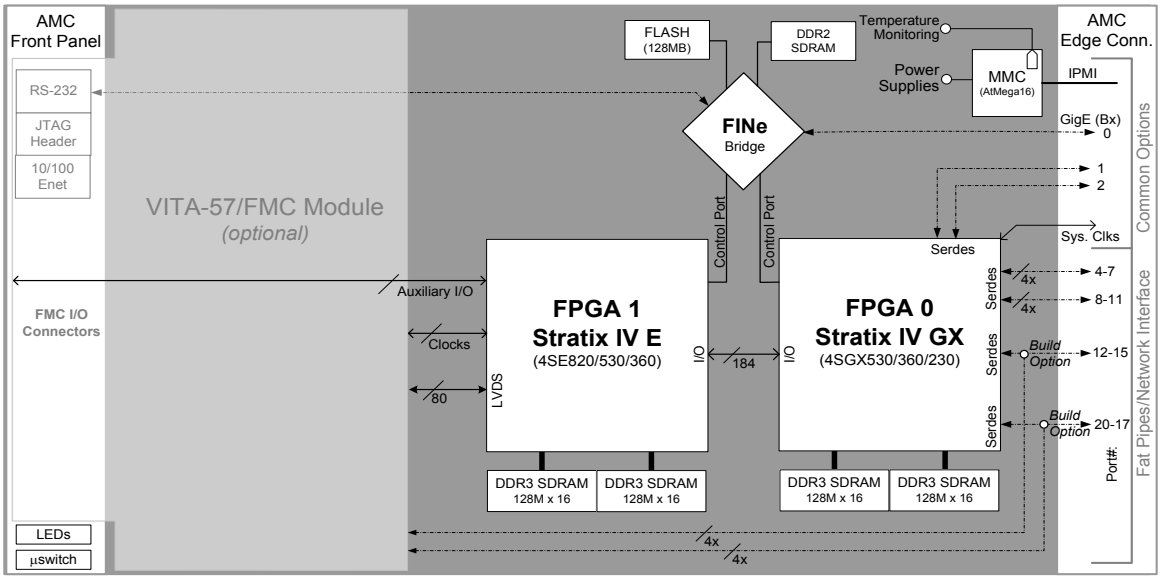
Development Platforms

- MicroTCA Rapid Development Platform

Accessory Boards

- BittWare GXBO breakout board for front panel I/O access
- BittWare AMBO breakout board for AMC I/O access

Figure 2: D4AM System Block Diagram



D4AM Ordering Options

D4AM-RW-AABB-CCDD-EF-GHIJKLLM

RW	Ruggedization Level 0U = Commercial (0C to 50C)*	AA	Altera Stratix IV GX FPGA Size 18 = Altera Stratix IV GX 180† 23 = Altera Stratix IV GX 230* 29 = Altera Stratix IV GX 290† 36 = Altera Stratix IV GX 360† 53 = Altera Stratix IV GX 530	BB	Altera Stratix IV GX Temperature Range & Speed C2 = Commercial temperature / speed grade 2 C3 = Commercial temperature / speed grade 3 C4 = Commercial temperature / speed grade 4* I2 = Industrial temperature / speed grade 2 I3 = Industrial temperature / speed grade 3 I4 = Industrial temperature / speed grade 4
CC	Altera Stratix IV E FPGA Size 36 = Altera Stratix IV E 360† 53 = Altera Stratix IV E 530* 82 = Altera Stratix IV E 820†	DD	Altera Stratix IV E Temperature Range & Speed C2 = Commercial temperature / speed grade 2 C3 = Commercial temperature / speed grade 3 C4 = Commercial temperature / speed grade 4* I2 = Industrial temperature / speed grade 2 I3 = Industrial temperature / speed grade 3 I4 = Industrial temperature / speed grade	E	Stratix IV GX DDR3 Size 0 = None 7 = 256 MBytes 8 = 512 MBytes*
F	Stratix IV E DDR3 Size 0 = None 7 = 256 MBytes 8 = 512 MBytes*	G	Fat Pipe 3 Configuration A = AMC* F = FMC	H	Fat Pipe 4 Configuration A = AMC* F = FMC
I	AMC Fat Pipe Decoupling Caps N = None A = Rx and Tx lanes 4-7, 8-11; Rx only lanes 12-15,20-17* B = Rx only, all lanes C = Rx and Tx lanes 4-7; Rx only all other lanes D = Tx only lanes 4-7,8-11; Rx only lanes 12-15, 20-17	J	Oscillator Configuration 0 = User Clock A 156.25 MHz, User Clock B 122.88 MHz* 1 = User Clock A 156.25 MHz, User Clock B 125 MHz	K	FMC Clock Direction 0 = M2C (mezzanine to carrier)* 1 = C2M (carrier to mezzanine)
LL	Front Panel 00 = No front panel M1 = Mid-size, VITA-57 cutout F1 = Full-size, VITA-57 cutout	M	Environmental Assembly 6 = RoHS 6/6* P = SnPb assembly		

* Default
† Contact Sky Blue or Zerif for availability.

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