S4AM (S4-AMC)

Altera Stratix® IV GX AdvancedMC with Optional VITA 57 FMC for I/O

- High density Altera Stratix IV GX
- BittWare's FINe™ III Host/Control Bridge provides control plane processing and interface
- VITA 57 FMC site for I/O and processing expansion
- Fully connected to AMC (16 ports SerDes, 4 ports GPIO)
- I/O includes 10/100/1000 Ethernet, SerDes, LVDS, RS-232, and JTAG

Based on Altera's Stratix IV GX FPGA, BittWare's S4-AMC (S4AM) is a mid- or full-size, single wide AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The S4AM features a high-density, low-power Altera Stratix IV GX FPGA designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable AMC. Providing enhanced flexibility is the VITA 57-compliant FMC site, which features 8 SerDes, 80 LVDS pairs, and 6 clocks directly to the FPGA. The board also provides an IPMI system management interface, a configurable 15-port AMC SerDes interface supporting a variety of protocols, and a front panel 4x SerDes interface supporting CPRI and OBSAI. Additionally, the board features 10/100 Ethernet, Gigabit Ethernet, 2 banks of DDR3 SDRAM, 2 banks of QDRII+ SRAM, and Flash memory for booting the FPGAs and FINe.

Altera Stratix IV GX FPGA

The Altera Stratix IV GX was specifically designed for serial I/O-based applications requiring high-density, reconfigurable logic. The Stratix IV GX provides 27 full-duplex, multi-gigabit transceivers, 24 of which are high-performance supporting PCI Express (Rev 1.0/2.0), 10GigE, GigE, Serial RapidIO (Rev 1.0/2.0), and SerialLite II standards. It contains up to 530k equivalent LEs, over 20 Mbits of embedded memory, and 1,024 embedded 18x18 multipliers.

Fat Pipes, Common Options, and I/O Interfaces

The Stratix IV GX FPGA interfaces to 3 ports (1, 2, & 3) in the AMC common options region, and 16 ports in the AMC fat pipes region (4 - 15, 17 - 20). These 19 ports provide a network data and control switch fabric interface on the AMC connector, with 12 supporting up to 6.25 GHz, 3 supporting up to 3.125 GHz, and the remaining 4 providing rear-panel GPIO. All AMC clocks are also connected to the Stratix IV GX. The front panel provides an additional 4 SerDes via an Infiniband-type connector, along with 10/100 Ethernet, 2 RS-232 ports, and a JTAG port for debug support.

VITA 57 FMC Site for Processing and I/O Expansion

The S4AM features an FMC (FPGA Mezzanine Card) site, which provides 8 high-performance SerDes and 80 LVDS, along with clocks, I^2C, JTAG, and reset connected to the Stratix IV. The site is based on the VITA 57 mezzanine standard for FPGA I/O, enabling designers to customize the S4AM to their individual needs with optional FMC I/O boards. A variety of I/O or processor FMCs are available integrated with the S4AM.

FINe™ III Host/Control Bridge

BittWare's FINe III Host/Control Bridge implements a complete control plane interface for the S4AM, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. Extensive software support is provided via BittWare's BittWorks Toolkit, which is tightly integrated with the FINe.

The FINe III provides GigE via the common options region, along with 10/100 Ethernet and an RS232 monitor port on the AMC front panel, and is connected to the FPGA via a local control bus.

Development Tools

BittWare offers complete software support for the S4AM with its BittWorks II software tools. The BittWorks II Toolkit is a collection of libraries and applications for BittWare's Stratix IV and V FPGA-based boards. Designed to make developing and debugging the applications for BittWare's boards easy and efficient, the Toolkit provides the glue between the host application and the hardware. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms.

Data Conversion and Processor FMC Options

A variety of VITA-57 FMCs are available to add I/O or Anemone processors to the S4AM's VITA-57 FMC site:

- 3F104: 4 channels 14-bit, 250 MSPS ADC
- 3F107: 8 channels 12-bit, 65 MSPS ADC
- 3F125: 1-4 channels 8-bit, up to 5 GSPS ADC
- 3F126: 1-4 channels 10-bit, up to 5 GSPS ADC
- 3F150: 2 channels, 14-bit, 250 MSPS ADC and 2 channels, 16-bit, 800 MSPS DAC
- 3F204: 1 - 4 channels 16-bit, up to 1 GSPS DAC
- SPFM: 4 front-panel SFP transceivers
- AAFM: 4 Anemone104 co-processors

Specifications

Board Architecture

FPGA

- Altera® Stratix® IV GX FPGA (4SGX230/530)
- 24 full-duplex, high-performance, multi-gigabit SerDes transceivers @ 6.25 GHz
- 3 full-duplex, multi-gigabit SerDes transceivers @ 3.125 GHz
- Over 530k equivalent LEs
- Over 20 Mbits of RAM
- Over 1,024 embedded multipliers

External Memory

- 2 banks of up to 1 GByte DDR3 SDRAM configured as x32
- 2 banks of up to 9 MBytes QDRII+ SRAM configured as x18
- 128 MBytes of Flash memory for booting FPGA and FINe

Fat Pipes Interface

- 12 ports (4 - 11, 20 - 17) @ up to 6.25 GHz, configurable to support PCI Express (Rev 1.0/2.0), Serial RapidIO (Rev 1.0/2.0), GigE, 10GigE/XAUI
- 4 ports (12 - 15) of GPIO

Common Options Interface

- BittWare's FINe™ III Host/Control Bridge providing GigE on port 0
- Ports 1, 2 & 3 via FPGA

Other AMC Edge Connections

- All AMC clocks brought to FPGA
- Module Management Control (MMC) Interface implementing IPMI for temperature monitoring and hot-swap support

AMC Front Panel I/O

- 4x SerDes via Infiniband-type connector (optional; not available with FMC)
- 10/100 Ethernet to FINe
- RS-232 port to Stratix IV GX
- RS-232 port to FINe
- JTAG debug interface to the Stratix IV GX

VITA 57 FMC Site

- VITA 57-compliant
- 8x high-performance SerDes to FPGA
- 80 LVDS pairs to FPGA
- 6 clocks to FPGA

Size

- AMC mid-size or full-size, single width format compatible with AMC.0 specification R2.0

Development Tools

BittWorks II Tools for Application Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks Porting kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems

FPGA Code Development

- Altera Quartus® II software

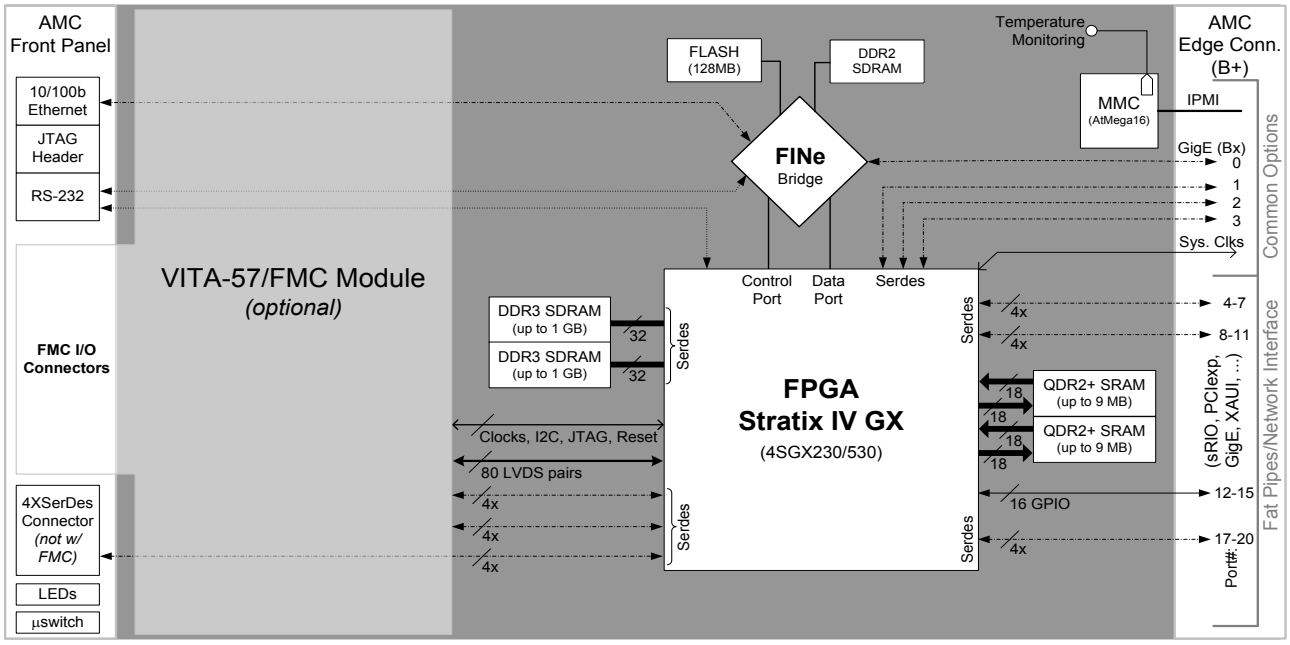
Development Platforms

- MicroTCA Rapid Development Platform

Accessory Boards

- BittWare GXBO breakout board for debug I/O
- BittWare AMBO breakout board for AMC I/O

Figure 3: S4AM System Block Diagram



S4AM Ordering Options

S4AM-RW-AABB-CDEFG-HHIJK-LM

RW	Ruggedization 0U = Commercial (0C to 50 C)*	AA	FPGA Size 23 = Altera Stratix IV GX 230 53 = Altera Stratix IV GX 530	BB	FPGA Speed Grade C2 = Commercial Speed Grade 2 C3 = Commercial Speed Grade 3 C4 = Commercial Speed Grade 4 I3 = Industrial Speed Grade 3 I4 = Industrial Speed Grade 4*	C	DDR3 Bank A Size 0 = None 8 = 512 MB* 9 = 1 GB†
D	DDR3 Bank B Size 0 = None 8 = 512 MB* 9 = 1 GB†	E	QDRII+ Bank A Size 0 = None* 2 = 9 MB†	F	QDRII+ Bank B Size 0 = None* 2 = 9 MB†	G	FINe Flash Size 6 = 128 MB*
HH	Front Panel 00 = No Front Panel† F1 = Full Size - VITA 57 Cutout* F2 = Full Size - SerDes Cutout M1 = Mid Size - VITA 57 Cutou† M2 = Mid Size - SerDes Cutout	I	Front Panel SerDes Connector 0 = Not Populated* 1 = Populated	J	Environmental Assembly 6 = RoHS 6/6* P = SnPb assembly	K	Factory Configuration 1 = BittWorks II compatible*
L	FMC Clock Direction 0 = M2C (mezzanine to carrier)* 1 = C2M (carrier to mezzanine)	M	AMC Port 1 Transceiver 0 = PMA only 1 = Standard*‡				

* Default
† Contact Sky Blue and Zerif for availability.
‡ This uses transceiver 7 from the FMC site.

Contact

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