S56X (S5-6U-VPX)

Intel Stratix® V GX/GS 6U VPX Board with two VITA-57 FMC I/O Sites

- Two High density Stratix V GX/GS FPGAs
- 800 MHz ARM® Cortex™-A8 control processor
- 48 multi-gigabit transceivers
- Two VITA 57 FMC sites for processing and I/O expansion
- Up to 8 GBytes on-board memory
- Board Management Controller for Intelligent Platform Management
- I/O includes: GigE, SerDes, LVDS, JTAG, RS-232

Configuration via Protocol (CvP) Supported

BittWare's S5-6U-VPX (S56X) is a 6U VPX card based on the high-bandwidth, power-efficient Intel Stratix V GX/GS FPGA. Designed for high-end applications, the Stratix V provides a high level of system integration and flexibility for I/O, routing, and processing. An ARM® Cortex™-A8 control processor provides a complete control plane interface; and a configurable 48-port multi-gigabit transceiver interface supports a variety of protocols, including Serial RapidIO, PCI Express, and 10GigE. The board features up to 8 GB of DDR3 SDRAM as well as Flash memory for booting the FPGAs. Providing additional flexibility are two VITA 57 FMC sites for enhancing the board's I/O and processing capabilities. The S56X also features a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management. All of these features combine to make the S56X a versatile and efficient solution for creating and deploying high-performance FPGA computing systems.

Intel Stratix V GX/GS FPGA

The Intel Stratix V FPGA is optimized for high-performance, high-bandwidth applications with integrated transceivers (up to 14.1 Gbps) supporting backplanes and optical modules. It supports 1.6 Tbps of serial switching capability and up to 3,926 18 x 18 variable precision multipliers. The Stratix V also provides PCI Express via a hard IP block and supports configuration by PCI Express using the existing PCI Express link in your application. For additional flexibility, the Stratix V supports transceiver and core reconfiguration on-the-fly while other portions of the design are running. The FPGA is supported by BittWare's FPGA Development Kit, which provides board support IP and integration.

I/O Interfaces

The S56X provides a variety of interfaces for high-speed serial I/O as well as debug support. The rear panel VPX interface includes GigE and 32 multi-gigabit transceiver channels to the Stratix V FPGAs. In addition, a Cyclone III FPGA is used to interface 48 LVDS and 20 GPIO from the VPX backplane to the Stratix V FPGAs. A utility header provides access to USB, RS-232, JTAG, and Ethernet interfaces for debug and programming support.

ARM® Cortex™-A8 Control Processor

An ARM® Cortex™-A8 control processor provides a complete control plane interface for the S56X, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. This is implemented in a 800 MHz TI AM3871 ARM processor running Linux. The ARM runs BittWorks server for full remote access via the BittWorks II Toolkit.

VITA 57 FMC Sites for Processing and I/O Expansion

The S56X features two FMC (FPGA Mezzanine Card) sites, which provide multi-gigabit transceivers and LVDS, along with clocks, I^2C, JTAG, and reset connected to the Stratix V. The sites are based on the VITA 57 mezzanine standard for FPGA I/O, enabling designers to customize the S56X to their individual needs with optional FMC I/O boards.

Board Management Controller

BittWare's S5 boards feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe, USB, or serial port. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

FPGA Development Kit

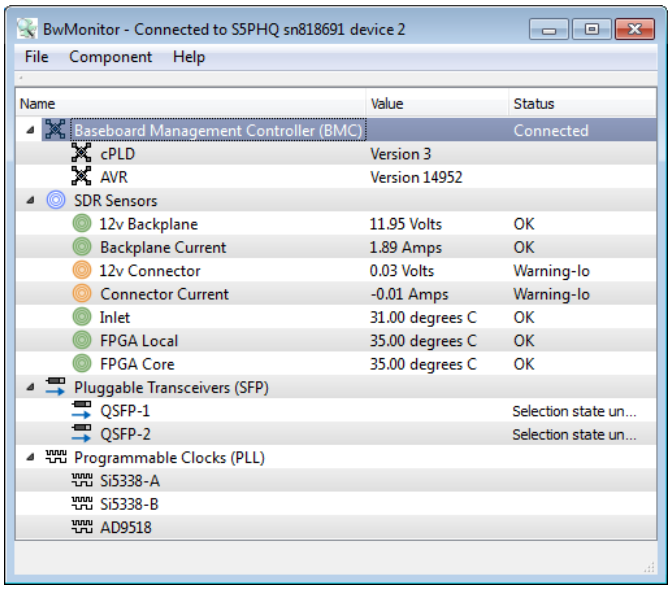
BittWare's FPGA DevKit provides FPGA board support IP and integration for BittWare's Intel FPGA-based COTS boards. The FDK includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR3, DDR2, QDR2/+, PCIe, 10GigE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.

Development Tools

BittWorks II Toolkit

BittWare offers complete software support for the S56X with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Stratix V FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe, Ethernet, or USB, providing a common API no matter the connection method.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

Data Conversion and Processor FMC Options

A variety of VITA-57 FMCs are available to add I/O to the S56X's VITA-57 FMC site:

- 3F104: 4 channels 14-bit, 250 MSPS ADC
- 3F107: 8 channels 12-bit, 65 MSPS ADC
- 3F125: 1-4 channels 8-bit, up to 5 GSPS ADC
- 3F126: 1-4 channels 10-bit, up to 5 GSPS ADC
- 3F150: 2 channels, 14-bit, 250 MSPS ADC and 2 channels, 16-bit, 800 MSPS DAC
- 3F204: 1 - 2 channels 16-bit, up to 1 GSPS DAC
- 3F230: 2 channels 14-bit, 5.6 GSPS DAC

S5-6U-VPX

Specifications

Board Architecture

FPGAs

- 2 Intel® Stratix® V GX/GS FPGAs
- 48 full-duplex, multi-gigabit transceivers @ up to 14.1 GHz
- Up to 952,000 logic elements per FPGA
- Up to 62 Mb on-chip memory (per FPGA)
- 1.4 Gbps LVDS performance
- Up to 3,926 18x18 variable-precision multipliers (per FPGA)
- Embedded HardCopy Blocks

External Memory

- Four banks of up to 2 GByte DDR3 SDRAM configured as x64
- Two 128 MByte banks of Flash memory for booting FPGA and ARM

ARM® Cortex™-A8 Control Processor

- 800 MHz ARM® Cortex™-A8 processor (TI AM3871) running Linux
- Control port interface to Stratix V FPGAs
- GigE, PCIe, and SATA interfaces
- Supports host- and Flash-based booting of Stratix V FPGAs
- Runs BittWorks server for full remote access via the BittWorks II Toolkit

VITA 57 FMC Sites

- Two VITA 57 FMC sites
- 8x multi-gigabit transceivers per site
- 80 LVDS pairs per site
- Clocks, I2C, JTAG, and reset

Rear Panel I/O

- 4 GigE (2 1000BaseT and 2 1000BaseX)
- 16 multi-gigabit transceivers from rear panel (VPX) to each Stratix V (32 total)
- 48 LVDS pairs (24 Tx and 24 Rx) and 20 GPIO from VPX backplane to the Stratix V FPGAs via a Cyclone III FPGA

Debug I/O (Utility Header)

- RS-232 ports to Stratix V and ARM
- Ethernet interface (10/100)
- JTAG debug interface to the Stratix V

Size

- VPX 6U single slot
- 233.35mm x 160mm

Board Management Controller

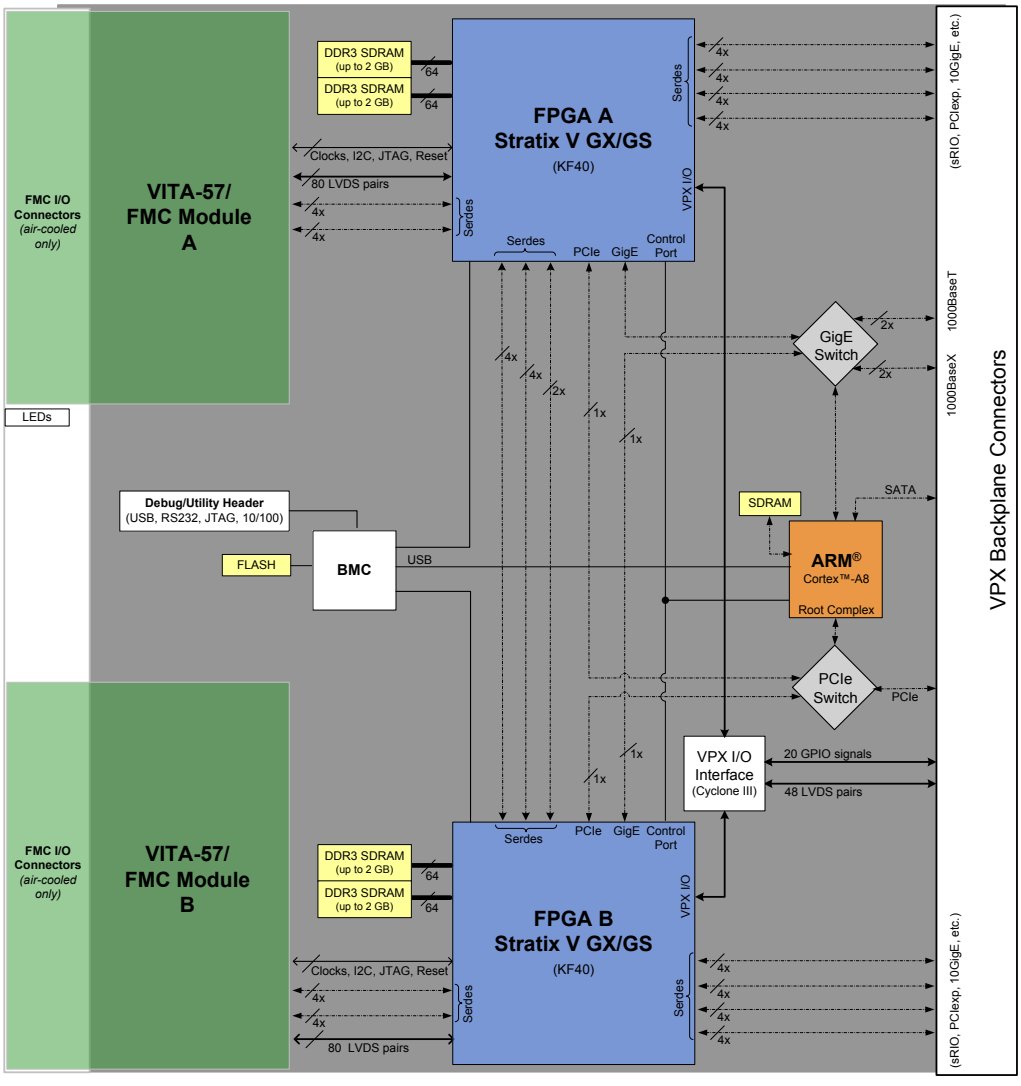
- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Development Tools

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks II Porting Kit - source code and prebuilt ports for porting the BittWorks II Toolkit to other operating systems

Figure 2: S56X System Block Diagram



FPGA Development Kit

- Physical interface components
- Board, I/O, and timing constraints
- Example Quartus projects
- Software components and drivers

FPGA Development

- Intel Quartus® II software

Accessory Boards

- BittWare BWBO breakout board for USB, JTAG, RS-232, and Ethernet access
- BittWare ACC-S56X-BORT rear transition module with QSFP, SFP, RJ-45, JTAG, PCIe x1, SATA, and Ref Clk input

S56X Ordering Options

S56X-RW-AAAAABCC-DE-0-GGGGGHII-JK-0-MN-OPQR-STUV-WX

RW	Ruggedization 0U = Commercial (0C to 50C)*
AAAAA	Cluster A S5 Family, HardIP, and Size 00000 = None GXEA3 = Stratix V GXEA3 GXEA4 = Stratix V GXEA4 GXEA5 = Stratix V GXEA5 GXEA7 = Stratix V GXEA7* GXEA9 = Stratix V GXEA9† GXEAB = Stratix V GXEAB† GSMD4 = Stratix V GSMD4 GSMD5 = Stratix V GSMD5 GSED6 = Stratix V GSED6† GSED8 = Stratix V GSED8†
B	Cluster A S5GXB Speed 1 = 14.1 Gbps 2 = 12.5 Gbps*‡ 3 = 8.5 Gbps
CC	Cluster A S5 Temp/Speed 00 = None I3 = Industrial Temperature Range, Speed Grade 3 I4 = Industrial Temperature Range, Speed Grade 4*
D	Cluster A DDR3 Bank A 0 = None 9 = 1GB A = 2 GB*
E	Cluster A DDR3 Bank B 0 = None 9 = 1GB A = 2 GB*
GGGGG	Cluster B S5 Family, HardIP, and Size (See options for AAAAA)
H	Cluster B S5GXB Speed 1 = 14.1 Gbps 2 = 12.5 Gbps*‡ 3 = 8.5 Gbps
II	Cluster B S5 Temp/Speed 00 = None I3 = Industrial Temperature Range, Speed Grade 3 I4 = Industrial Temperature Range, Speed Grade 4*
J	Cluster B DDR3 Bank A 0 = None 9 = 1GB A = 2 GB*
K	Cluster B DDR3 Bank B 0 = None 9 = 1GB A = 2 GB*
M	Rear Panel Analog Connectors 0 = Not Populated 1 = Populated*
N	VPX I/O Configuration 1 = Standard
O	ClusterA Reference Clock A Frequency 0 = 156.25MHz*
P	Cluster B Reference Clock A Frequency 0 = 156.25MHz*
Q	Reference Clock B Frequency 5 = 322.265625MHz*
R	Reference Clock C Frequency 0 = 125 MHz*
S	VPX Rear Panel Connectors 1 = Standard (P0 - P4 installed)*
T	VPX Key Position 1 1 = 0 Degrees 2 = 45 Degrees 3 = 90 Degrees 7 = 270 Degrees 8 = 315 Degrees* 9 = Unkeyed
U	VPX Key Position 2 1 = 0 Degrees 2 = 45 Degrees 3 = 90 Degrees 7 = 270 Degrees 8 = 315 Degrees 9 = Unkeyed*
V	VPX Key Position 3 1 = 0 Degrees 2 = 45 Degrees 3 = 90 Degrees 7 = 270 Degrees 8 = 315 Degrees 9 = Unkeyed*
W	Mechanical 1 = Standard Air Cooled Panel* 2 = 1" Pitch Air Cooled Panel
X	Environmental Assembly P = SnPb assembly*

* Default

† Contact Sky Blue or Zerif for availability.

‡ On GXEAB devices, the Stratix V GXB speed is 11.2 Gbps.

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