BittWare
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Development Tools
Custom Solutions
Board Platforms
Technology Partners
Integrated Platforms

S5-PCIe-F

Intel Stratix® V GX/GS PCIe Board with VITA 57 FMC Site

- High density Intel Stratix V GX/GS

- PCIe x8 interface supporting Gen1, Gen2, or Gen3

- VITA 57 FMC site for I/O with full High Pin Count support

- Four SATA connectors, up to 6 Gbps each

- Timestamping support

- Memory options:

  - up to 16 GBytes of DDR3 SDRAM with ECC

  - up to 1 GByte RLDRAM3

  - up to 72 MBytes QDRII+

- Board Management Controller for Intelligent Platform Management

- Utility I/O includes: USB 2.0, RS-232, and JTAG

B ittWare's S5-PCIe-F (S5PE-F) is a PCIe x8 card based on the high-bandwidth, power-efficient Intel Stratix V GX/GS FPGA. Designed for high-end applications, the Stratix V provides a high level of system integration and flexibility for I/O, routing, and processing. The S5PE-F is a flexible and efficient solution for high-performance network and signal processing, signal processing, and data acquisition.

The board provides up to 16 GB of DDR3 SDRAM with optional error-correcting codes (ECC) as well as options for up to 1 GByte RLDRAM3 and up to 72 MBytes QDRII+. Providing additional flexibility is an optional VITA 57 FMC site for enhancing the board's I/O and processing capabilities, making it ideal for analog I/O and processing. The S5PE-F also features a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management.

Intel Stratix V GX/GS FPGA
The Intel Stratix V FPGA is optimized for high-performance, high-bandwidth applications with integrated transceivers (up to 14.1 Gbps) supporting backplanes and optical modules. It supports 1.6 Tbps of serial switching capability and up to 3,926 18 x 18 variable precision multipliers. The Stratix V also provides PCI Express x8 via a hard IP block and supports configuration by PCI Express using the existing PCI Express link in your application. For additional flexibility, the Stratix V supports transceiver and core reconfiguration on-the-fly while other portions of the design are running. The FPGA is supported by BittWare's FPGA Development Kit, which provides board support IP and integration.

VITA 57 FMC and Expansion Sites for Processing and I/O
The S5PE-F features an FMC (FPGA Mezzanine Card) site, which provides high-performance SerDes and LVDS, along with clocks, I²C, and JTAG connected to the Stratix V. The site is based on the VITA 57 mezzanine standard for FPGA I/O, enabling designers to customize the S5PE-F to their individual needs with optional FMC I/O boards. A variety of I/O or processor FMCs are available integrated with the S5PE-F.

An additional expansion site provides 10 SerDes and general-purpose I/O to the Stratix V. The site can be used for board-to-board communication, general-purpose I/O, or additional optical links.

I/O Interfaces
The S5PE-F provides a variety of interfaces for high-speed serial I/O as well as debug support. Four SerDes lanes are available via four SATA connectors to connect external storage devices with the FPGA or provide direct board-to-board communication. The x8 PCIe interface provides 8 SerDes lanes to the Stratix V FPGA. USB 2.0, RS-232, and JTAG interfaces are available for debug and programming support. The board also supports timestamping with provision for a 1 PPS and reference clock input as well as RS-232 for connection to GPS or other time sources.

Memory and SODIMM Options
The S5PE-F features an extremely flexible memory configuration, with two SODIMM sites that support DDR3 SDRAM, RLDRAM3, and QDRII+. Memory card options include the following: up to 8 GBytes of DDR3 with optional error-correcting codes (ECC); up to 36 MBytes QDRII+ (2 banks x18); or up to 512 MBytes RLDRAM3 (2 banks x18). RLDRAM3 is a high-performance memory targeted for systems requiring high bandwidth and low latency. The board also provides Flash memory for storing multiple FPGA images.

Board Management Controller

BittWare's S5 boards feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I²C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe, USB, or serial port. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

FPGA Development Kit

BittWare's FPGA Development Kit (FDK) provides FPGA board support IP and integration for BittWare's Intel FPGA-based COTS boards. The FDK includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR3, DDR2, QDR2/+, PCIe, 10GigE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.
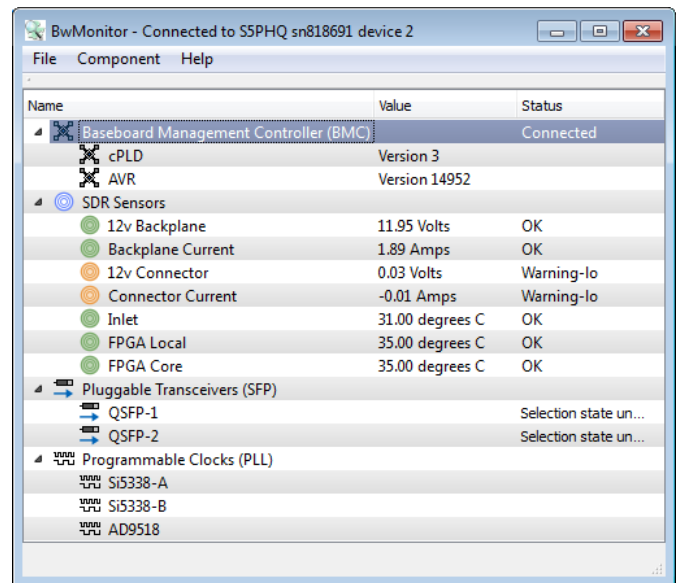
Development Tools

BittWorks II Toolkit

BittWare offers complete software support for the S5PE-F with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Stratix V FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe, Ethernet, or USB, providing a common API no matter the connection method.

BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

Data Conversion and Processor FMC Options

A variety of VITA-57 FMCs are available to add I/O to the S5PE-F VITA-57 FMC site:

- 3F104: 4 channels 14-bit, 250 MSPS ADC
- 3F107: 8 channels 12-bit, 65 MSPS ADC
- 3F125: 1-4 channels 8-bit, up to 5 GSPS ADC
- 3F126: 1-4 channels 10-bit, up to 5 GSPS ADC
- 3F150: 2 channels, 14-bit, 250 MSPS ADC and 2 channels, 16-bit, 800 MSPS DAC
- 3F204: 1 - 2 channels 16-bit, up to 1 GSPS DAC
- 3F230: 2 channels 14-bit, 5.6 GSPS DAC

S5-PCIe-F

S5PE-F Specifications

BOARD SPECIFICATIONS

FPGA

- Intel® Stratix® V GX/GS FPGA
- 32 full-duplex, high-performance, multi-gigabit SerDes transceivers @ up to 14.1 Gbps
- Up to 952,000 logic elements (LEs) available
- Up to 62 Mb of embedded memory
- 1.4 Gbps LVDS performance
- Up to 3,926 18x18 variable-precision multipliers
- Embedded HardCopy Blocks

Memory

- 2 SODIMM sites supporting DDR3, RLDRAM3, or QDRII+
- Up to 256 MBytes of Flash memory for booting PGA

PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

VITA 57 FMC Site (optional)

- Full High Pin Count support
- 10x high-performance SerDes
- 80 bi-directional LVDS
- Clocks, I²C, and JTAG

I/O and Debug Connectors

- Serial ATA: 4 connectors direct to FPGA, 6 Gbps
- Timestamp header: 1 PPS input, reference clock input, and RS-232

- USB 2.0: for debug and programming FPGA and Flash
- Debug Utility header: RS-232 and JTAG to Stratix V

Expansion Site

- 10x high-performance SerDes
- General-purpose I/O

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- Full-length, standard-height PCIe slot card
- x16 mechanical, x8 electrical
- 312mm x 111.15mm
- Max. component height: 14.47mm (single slot), 34.79mm (dual slot)

OPTIONAL SODIMMs*

DDR3: x72 w/ECC

- Up to 8 GB per SODIMM (DDR3-1600)

RLDRAM3: 2x banks of x18

- 2x (32 M x 18): 128 MB per SODIMM
- 2x (64 M x 18): 256 MB per SODIMM
- 2x (128M x 18): 512 MB per SODIMM

QDRII+: 2x banks of x18

- 2x (4 MB x 18): 18 MB per SODIMM
- 2x (8 MB x 18): 36 MB per SODIMM

Development Tools

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; source code porting kit also available

FPGA Development Kit

- Physical interface components
- Board, I/O, and timing constraints
- Example Quartus projects
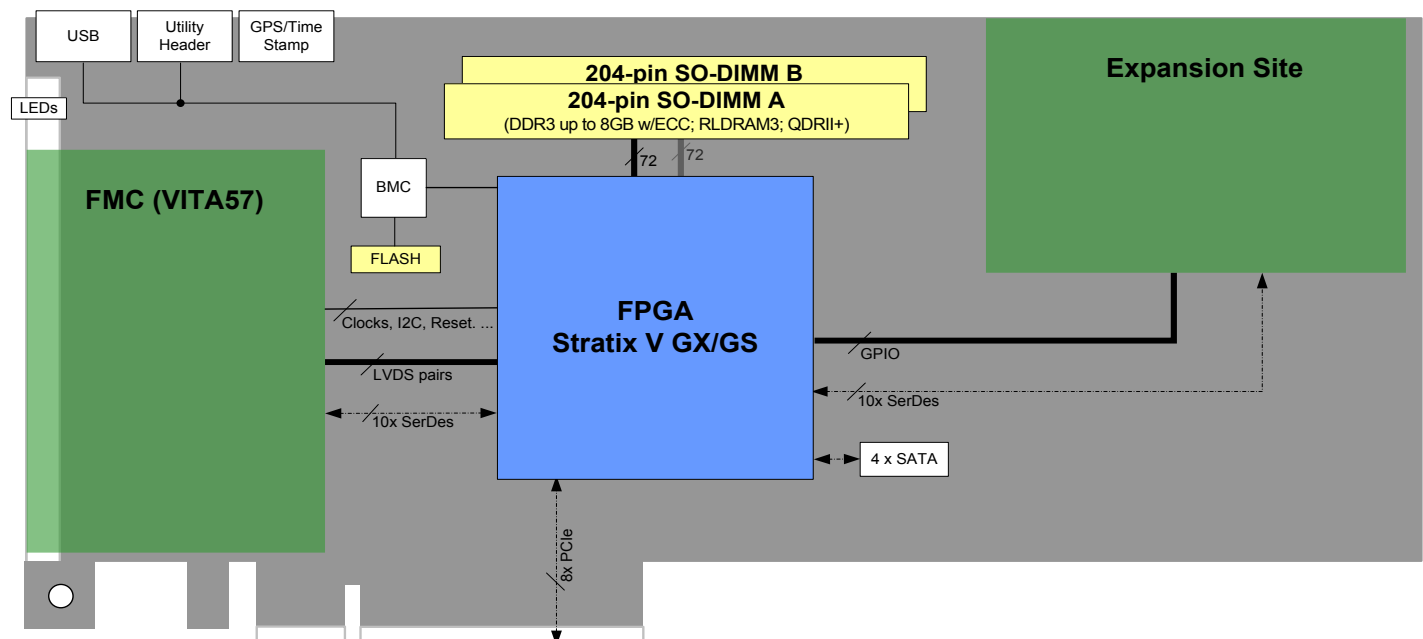- Software components and drivers

FPGA Development

- Intel Quartus® II software

Accessory Boards

- BittWare BWBO breakout board for JTAG and RS-232 access

* Combining two different SODIMM types on the S5PE-F places a restriction on using the full High Pin Count of the FMC site. If both SODIMM sites are populated with the same type of SODIMM, there is no restriction.

Figure 2: S5PE-F System Block Diagram

S5PE-F Ordering Options

S5PEF-RW-AAAAABCC-DDEE-FGH-IJK-L

Code	Description
RW	**Ruggedization** 0U = Commercial (0C to 50C)*
AAAAA	**Stratix V Family, HardIP, and Size** GXEA3 = Stratix V GXEA3† GXEA4 = Stratix V GXEA4† GXEA5 = Stratix V GXEA5† GXEA7 = Stratix V GXEA7† GXEA9 = Stratix V GXEA9† GXEAB = Stratix V GXEAB* GSMD4 = Stratix V GSMD4† GSMD5 = Stratix V GSMD5† GSED6 = Stratix V GSED6† GSED8 = Stratix V GSED8*
B	**Stratix V GXB Speed** 1 = 14.1 Gbps 2 = 12.5 Gbps*‡ 3 = 8.5 Gbps
CC	**Stratix V Temp/Speed** C1= Commercial Temperature Range, Speed Grade 1 C2= Commercial Temperature Range, Speed Grade 2* C3= Commercial Temperature Range, Speed Grade 3
DD	**Cluster A SODIMM** 00 = None D1 = DDR3 2GB x72 D2 = DDR3 4GB x72 D3 = DDR3 8GB x72* Q1 = QDRII+ 18MB 2x18 Q2 = QDRII+ 36MB 2x18 R1 = RLDRAM3 128MB 2x18 † R2 = RLDRAM3 256MB 2x18 † R3 = RLDRAM3 512MB 2x18 †
EE	**Cluster B SODIMM** 00 = None D1 = DDR3 2GB x72 D2 = DDR3 4GB x72 D3 = DDR3 8GB x72* Q1 = QDRII+ 18MB 2x18 Q2 = QDRII+ 36MB 2x18 R1 = RLDRAM3 128MB 2x18 † R2 = RLDRAM3 256MB 2x18 † R3 = RLDRAM3 512MB 2x18 †
F	**Front Expansion Site** 1 = FMC
G	**Rear Expansion Site** 0 = Not installed 1 = Installed
H	**Oscillator** S = Standard T = TCXO
I	**Heatsink** B = FPGA Fansink* E = FPGA Heatsink
J	**Mechanical Options** 1 = 1 slot standard 2 = 2 slot standard
K	**Misc. Configuration** 0 = Standard
L	**Environmental Assembly** 6 = RoHS 6/6*

* Default
† Contact Sky Blue and Zerif for availability.
‡ On GXEAB devices, the Stratix V GXB speed is 11.2 Gbps.

International Distributors