BittWare
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Development Tools
Board Platforms
Integrated Platforms
Custom Solutions
Technology Partners

XUPPL4

Xilinx UltraScale+ Low-Profile PCIe Board
with Dual QSFP and DDR4

XILINX
ALLIANCE PROGRAM

- Xilinx Virtex UltraScale+ VU3P
- PCIe x16 interface supporting Gen1, Gen2, or Gen3
- Two QSFP28 cages for 2x 100GbE, 2x 40GbE, 8x 25GbE, or 8x 10GbE
- Memory: up to 32 GBytes of DDR4 SDRAM with ECC (x72)
- Board Management Controller for Intelligent Platform Management
- Precision timestamping support
- Utility I/O: USB 2.0

BittWare's XUPPL4 is a low-profile PCIe x16 card based on the Xilinx Virtex UltraScale+ FPGA. The UltraScale+ devices deliver high-performance, high-bandwidth, and reduced latency for systems demanding massive data flow and packet processing. The board offers up to 32 GBytes of memory, sophisticated clocking and timing options, and two front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE. The XUPPL4 also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUPPL4 ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

Xilinx Virtex UltraScale+ FPGA

The Xilinx UltraScale+ FPGAs are built on 16 nm process technology using 16FF+ FinFET 3D transistors to offer higher performance per watt than previous generations. Virtex UltraScale+ VU3P devices feature up to 40x 32.75 Gbit/s transceivers, which enable 400GbE, 100GbE, and 25GbE. The UltraScale+ FPGAs offer programmable system integration with over 115 Mb of on-chip memory, integrated 100G Ethernet MAC with RS-FEC and 150G Interlaken cores, and IP blocks for PCIe Gen3 x16 and Gen4 x8. Up to 2,280 DSP slices provide high-level DSP compute performance.

I/O Interfaces

The XUPPL4 provides a variety of interfaces for high-speed serial I/O as well as debug support. Two QSFP28 cages are available on the front panel, each supporting 100GbE, 40GbE, four 25GbE, or four 10GbE channels, for a total of up to 200 Gbps of bandwidth. The QSFP channels are connected directly to the UltraScale+ FPGA via 8 transceivers. The QSFP cages can optionally be adapted for SFP+.

A Gen3 x16 PCIe interface connects to the FPGA via 16 transceivers. A USB 2.0 interface provides BMC access. The board also supports precision timestamping with provision for a 1 PPS and reference clock input and output.

Memory

The XUPPL4 features up to 32 GBytes DDR4 on-board. Additional on-board memory includes Flash with factory default and support for multiple FPGA images.

Board Management Controller

The XUPPL4 features an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

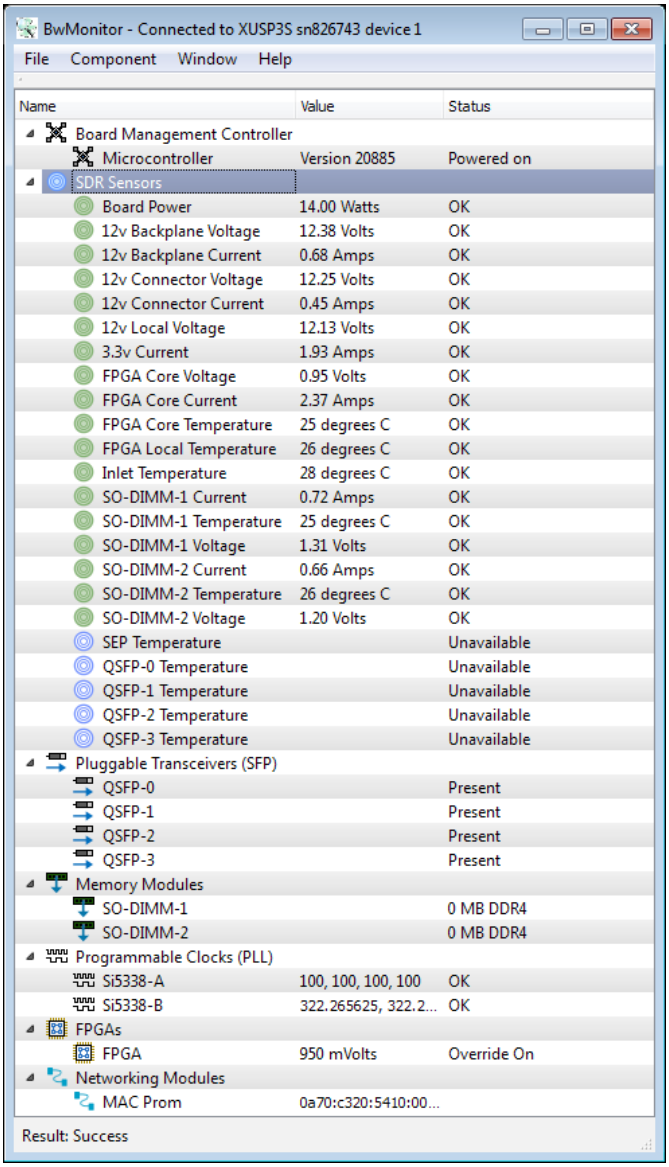
Development Tools

BittWorks II Toolkit

BittWare offers complete software support for the XUPPL4 with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Xilinx UltraScale+ FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

FPGA Example Projects

BittWare offers FPGA example projects to provide board support IP and integration for its Xilinx FPGA-based boards. The example projects easily integrate into existing FPGA development environments and illustrate how to move data between the board's different interfaces. Available example projects include the following: PCIe Gen3x16 Base Project, PCIe DMA, DDR4, and SerDes (iBERT). All examples are available for download on BittWare's developer website.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

Specifications

Board Specifications

FPGA

- Virtex UltraScale+ VU3P
- 24x GTY transceivers at 32.75 Gbps
- 862K logic elements
- 115 Mb of embedded memory
- 2 integrated PCIe cores
- 2,280 DSP slices with 27x18 multipliers

On-Board Memory

- Two banks of up to 16 GB DDR4 (x72)
- Flash memory for booting FPGA

PCIe Interface

- x16 Gen1, Gen2, Gen3 interface direct to FPGA

USB Header

- Micro USB port (USB 2.0) for BMC access and programming Flash

QSFP Cages

- 2 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 8 transceivers
- Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

Timestamping (Optional)

- 1 PPS input/output
- Reference clock input/output

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0
- Voltage overrides

Size

- Low profile (Half-height, half-length) PCIe slot card; x16 mechanical

Development Tools

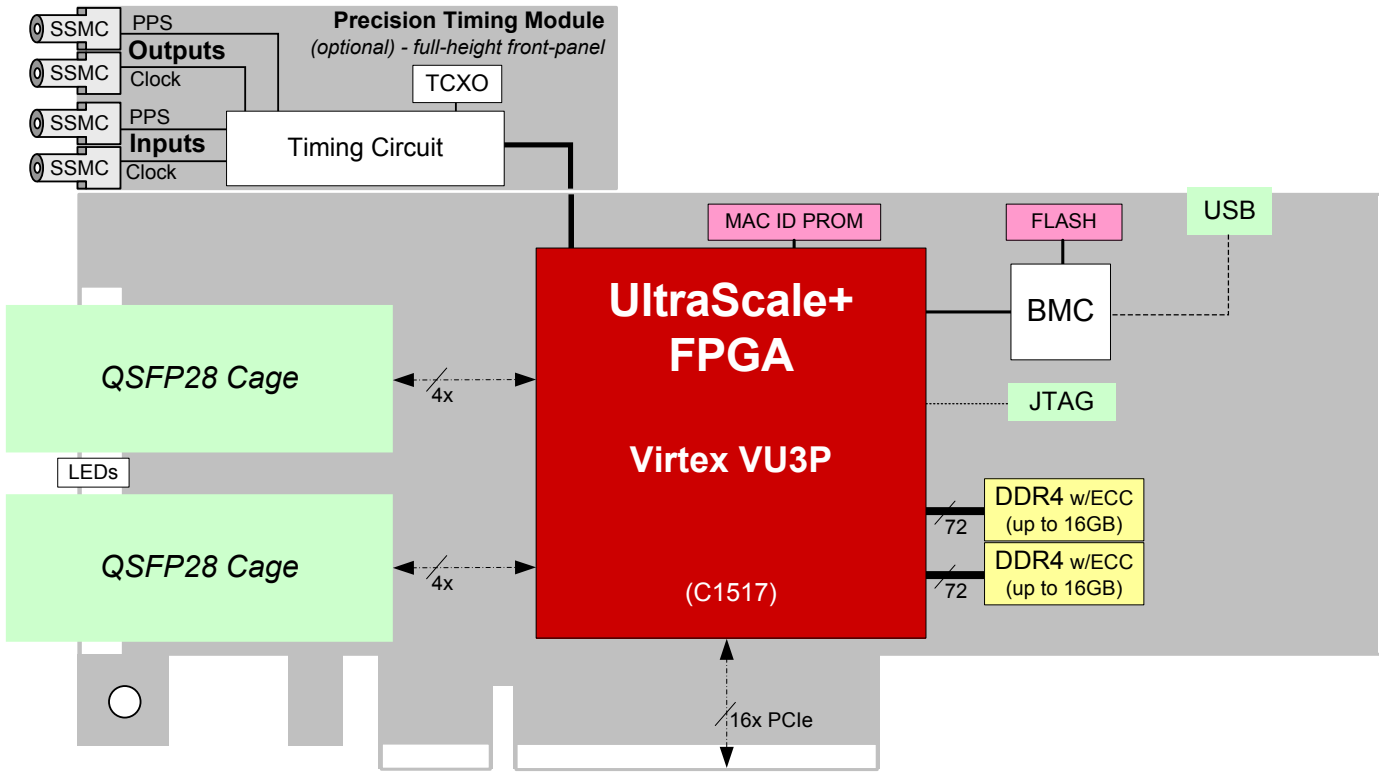
System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

FPGA Development

- FPGA Example Projects
  - PCIe Gen3x16 Base Project
  - PCIe DMA
  - DDR4
  - SerDes (iBERT)
- Xilinx Tools
  - Vivado® Design Suite
  - USB to JTAG converter

Figure 2: XUPPL4 System Block Diagram



XUPPL4 Ordering Options

XUPPL4-RW-ABBBBCD-EF-GIJKL-MO

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)*
A	**UltraScale Printed Wiring Board** E = Optimized for VU3P FPGA*
BBBB	**FPGA Type and Size** 03VP = Virtex VU3P*
C	**FPGA Core Speed Grade** 1 = Slower 2 = Standard* 3 = Faster
D	**FPGA Temperature Range** E = Extended (Tj = 0 to +100C)*
E	**DDR4 Bank A** 0 = None 2 = 4GB* 3 = 8GB 4 = 16GB
F	**DDR4 Bank B** 0 = None 2 = 4GB* 3 = 8GB 4 = 16GB
G	**Oscillator** S = Standard*
I	**QSFP Configuration** 2 = 2 QSFP cages*
J	**JTAG** 1 = Installed*
K	**Front Panel Configuration** F = Full-height H = Half-height* T = Full-height with Precision Timing Module
P	**Heatsink** A = Active*
Q	**Misc. Configuration** 0 = Default*
R	**Assembly** 6 = RoHS 6/6*

* Default.

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