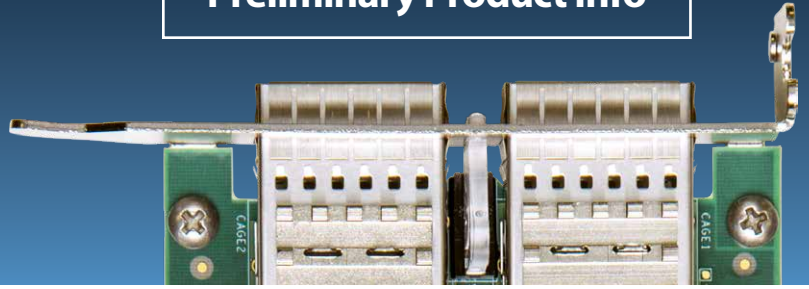**BittWare**
a **molex** company

XUPSV2
PCIe FPGA Board

Low-profile PCIe with Virtex VU9P

BittWare's XUPSV2 is a low-profile PCIe card featuring a very large FPGA — the Xilinx Virtex UltraScale+ VU9P, which offers up to 2.5 million logic elements. The board features 2x 40/100 Gbps Ethernet (8x 25/10 GbE through breakout cables) for high-speed networking along with up to 16GBytes of DDR4 SDRAM.

The XUPSV2 is designed with BittWare's Spider platform, which is a low-profile PCIe platform optimized for thermal performance. The Spider platform combines a low-profile PCIe form-factor for high density and a robust passive heatsink option designed for servers.
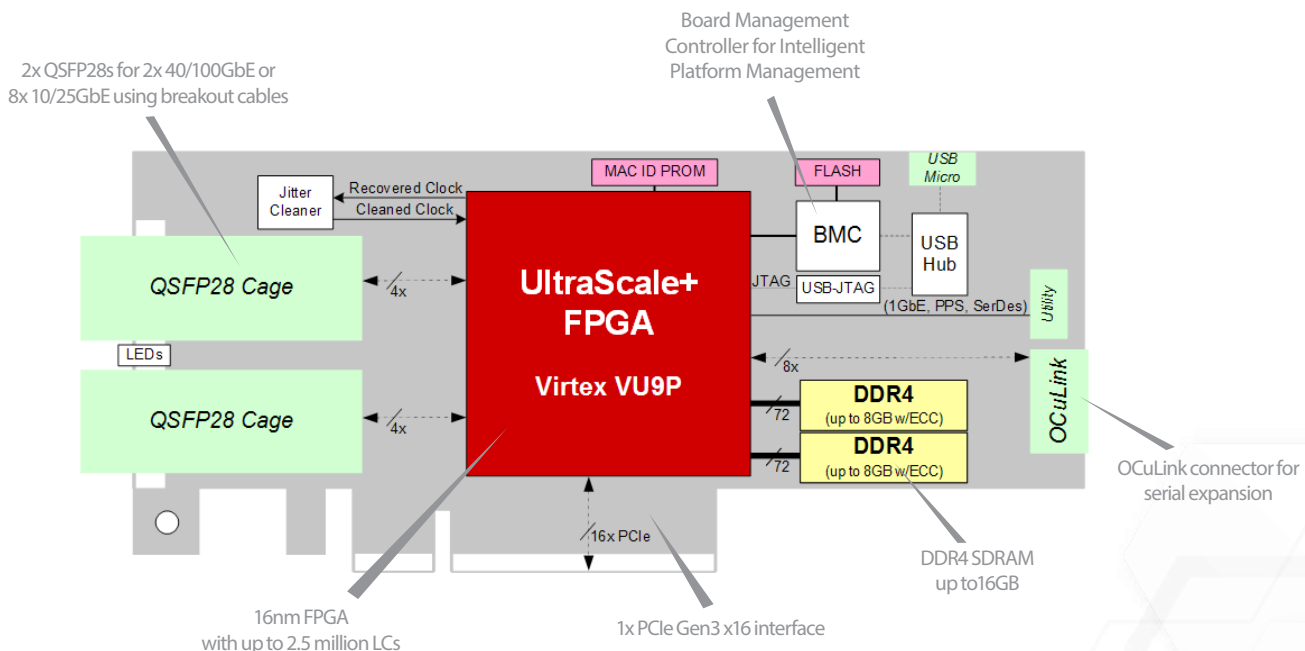
Built on **BittWare**

SPIDER PLATFORM

Spider Platform: designed for high-performance passive cooling in servers

key features

2 QSFPs
for
**2x 100 GbE or
8x 10/25 GbE**

Single Slot
Large FPGA on
small form-factor

Up to VU9P FPGA:
**2.5 million LCs
270Mb UltraRAM**
FPGA by Xilinx

2x QSFP28s for 2x 40/100GbE or
8x 10/25GbE using breakout cables

Board Management
Controller for Intelligent
Platform Management

MAC ID PROM

FLASH

USB Micro

Jitter Cleaner

Recovered Clock
Cleaned Clock

BMC

USB Hub

USB-JTAG

JTAG

(1GbE, PPS, SerDes)

Utility

QSFP28 Cage

4x

**UltraScale+
FPGA**

Virtex VU9P

LEDs

QSFP28 Cage

4x

8x

OCuLink

DDR4
(up to 8GB w/ECC)

DDR4
(up to 8GB w/ECC)

72

72

16x PCIe

16nm FPGA
with up to 2.5 million LCs

1x PCIe Gen3 x16 interface

DDR4 SDRAM
up to16GB

OCuLink connector for
serial expansion

High-Speed Networking and I/O

The XUPSV2 is enabled for high-speed networking with two front panel QSFP+ cages, each supporting 40/100GbE or four 10/25GbE channels. A jitter cleaner is provided for using recovered clocks to support Synchronous Ethernet.

Serial expansion is available through an OCuLink connector (8x 25Gbps) that can be connected to another XUPSV2 or other devices, including IBM's POWER9 via OpenCAPI. A utility header provides a PPS input, 10MHz reference clock, and 2 FPGA transceivers (could be used to support 1GbE). A USB micro port allows USB access to the BMC, USB-to-JTAG, and a USB UART for debug and programming support.

System Management

For system management, the XUPSV2 is equipped with a Board Management Controller (BMC), which accepts IPMI 2.0 commands. Use it along with BittWare's BittWorks II Toolkit to program the FPGA Flash over USB, monitor board power and temperature, re-program the onboard clocks, and adjust FPGA core voltage. The BMC monitors critical temperatures, voltages, and current and will shut the board down to prevent damage. Recovery from shutdown is also supported, without the need to cycle system power.

BittWorks II Toolkit

BittWare offers complete software support for the XUPSV2 with its BittWorks II software tools. The BittWorks II Toolkit is a suite of development tools that serves as the main interface between the BittWare board and the host system. The Toolkit includes drivers, libraries, utilities, and example projects for accessing, integrating, and developing applications for the BittWare board.

FPGA Examples

BittWare provides FPGA board support IP to simplify integration and development. These example projects illustrate how to move data between the board's different interfaces and are designed to integrate easily with the Xilinx Vivado tools. All examples are available for download on BittWare's developer website. they flow through and then any number of Actions are applied based on those labels.

BwMonitor

Name	Value	Status
Board Management Controller		
Microcontroller	Version 28591	Powered on
SDR Sensors		
Board Power	224 Watts	OK
12v Cable Current	17.69 Amps	OK
12v Cable Voltage	11.60 Volts	OK
12v PCIe Current	1.00 Amps	OK
12v PCIe Voltage	11.60 Volts	OK
3.3V MP Voltage	3.3 Volts	OK
3.3V MP Current	2.36 Amps	OK
3.3V MP2 Voltage	3.3 Volts	OK
3.3V MP2 Current	0.18 Amps	OK
DIMM12 Voltage	1.19 Volts	OK
DIMM12 Current	-0.01 Amps	OK
FPGA Core Voltage	0.84 Volts	OK
FPGA Core Current 0	149.53 Amps	OK
FPGA Supply Die Temp	83 degrees C	OK
FPGA Supply Inductor Te...	77 degrees C	OK
FPGA Supply Inductor Te...	77 degrees C	OK
FPGA Slave Supply Temp 0	85 degrees C	OK
FPGA Slave Supply Temp 1	90 degrees C	OK
FPGA Core Temperature	53 degrees C	OK
Board Temperature	46 degrees C	OK
Vcc AUX Voltage	1.76 Volts	OK
Vcc AUX Current	0.72 Amps	OK

Live board power/temperature display is included as part of Toolkit Lite

Board Specifications

FPGA	• Virtex UltraScale+ VU9P • 40x GTY transceivers at 32.75 Gbps • Up to 2.5 million logic elements • Up to 345 Mb of embedded memory • Integrated PCIe cores • Up to 6,840 DSP slices with 27x18 multipliers
On-board memory	• 2x 8GByte banks of DDR4 with ECC • Flash memory for booting FPGA
PCIe interface	x16 Gen1, Gen2, Gen3 interface direct to FPGA
Utility header	• 1 PPS and 10MHz ref clk • 2 FPGA transceivers (could be used to support 1GbE)
USB Micro	USB access to BMC, USB-JTAG, USB-UART
OCuLink	• OCuLink connector on rear edge connected to FPGA via 16x GTY transceivers • Provides 200Gbps board-to-board bandwidth
QSFP cages	• 2 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 8x transceivers • Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE

Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • I²C bus access • USB 2.0 • Voltage overrides
Cooling	Air-cooled Spider platform, passive or active
Size	• Low profile (Half-height, half-length) PCIe slot card; x16 mechanical • 168mm x 68.9mm

Development Tools

System development	BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
FPGA development	• FPGA Examples - example Vivado projects • Xilinx Tools - Vivado® Design Suite

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