BittWare a molex company

XUPVV4
PCIe FPGA Board

UltraScale+ PCIe board with VU13P

XILINX

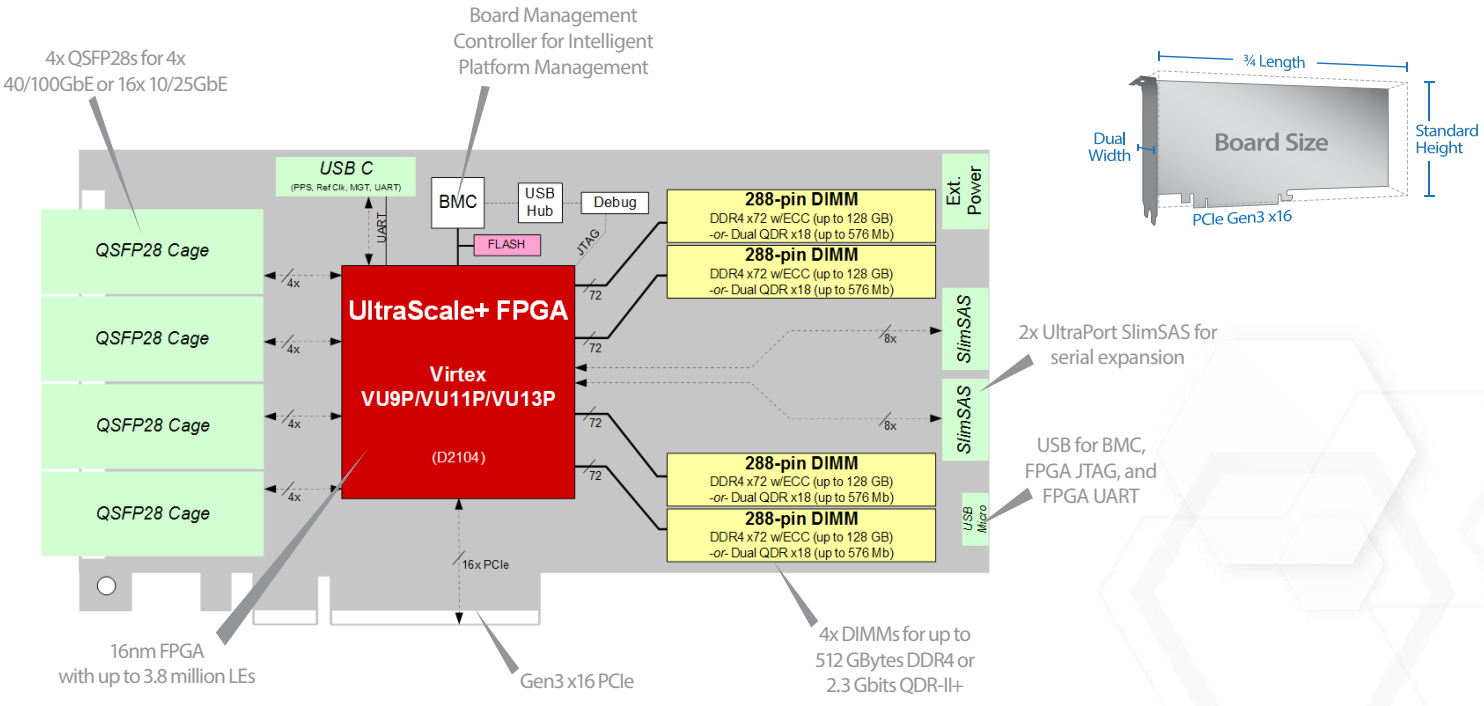
BittWare's XUPVV4 is an UltraScale+ VU13P FPGA-based PCIe card, ideal for high-density datacenter applications. The Xilinx UltraScale+ VU13P FPGA gives designers incredible performance potential, with 3.8M logic elements —yet with a power density that makes thermal management difficult. The XUPVV4 meets this challenge with BittWare's Viper platform, supporting large FPGA loads, up to 512 GBytes DDR4, and 4x 100 Gbps Ethernet.

BittWare's Viper platform uses advanced computer flow simulation to drive the physical board design in a thermals first approach, including the use of heat pipes, airflow channels, and arranging components to maximize the limited available airflow in a server. The XUPVV4 features air cooling by default, but liquid cooling is also available. The board features the D2104 lidless package from Xilinx—allowing the heat pipes to contact the die directly, instead of through the heat spreader lid.

Xilinx VU13P FPGA: lidless package is used by BittWare's Viper thermal management for enhanced cooling performance

key features

- **4x 100GbE** via 4 QSFP28
- **Air** or **Liquid** Cooled
- VU13P FPGA: **3.8 million LCs** FPGA by Xilinx



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High-Speed Networking and I/O

The XUPVV4 is enabled for high-speed networking with four front panel QSFP+ cages, each supporting 40/100GbE or four 10/25GbE channels. Serial expansion is available through two UltraPort SlimSAS connectors (16x 24Gbps) that can be connected to a second PCIe interface, another XUPVV4, or other devices, including IBM's POWER9 via OpenCAPI. A utility header provides a 1GbE interface, a PPS input, and a USB interface for debug and programming support.

System Management

For system management, the XUPVV4 is equipped with a Board Management Controller (BMC), which accepts IPMI 2.0 commands. Use it along with BittWare's BittWorks II Toolkit to program the FPGA Flash over USB, monitor board power and temperature, re-program the onboard clocks, and adjust FPGA core voltage. The BMC monitors critical temperatures, voltages, and current and will shut the board down to prevent damage. Recovery from shutdown is also supported, without the need to cycle system power.

BittWorks II Toolkit

BittWare offers complete software support for the XUPVV4 with its BittWorks II software tools. The BittWorks II Toolkit is a suite of development tools that serves as the main interface between the BittWare board and the host system. The Toolkit includes drivers, libraries, utilities, and example projects for accessing, integrating, and developing applications for the BittWare board.

FPGA Examples

BittWare provides FPGA board support IP to simplify integration and development. These example projects illustrate how to move data between the board's different interfaces and are designed to integrate easily with the Xilinx Vivado tools. All examples are available for download on BittWare's developer website.

BwMonitor

Name	Value	Status
Board Management Controller		
Microcontroller	Version 28591	Powered on
SDR Sensors		
Board Power	224 Watts	OK
12v Cable Current	17.69 Amps	OK
12v Cable Voltage	11.60 Volts	OK
12v PCIe Current	1.00 Amps	OK
12v PCIe Voltage	11.60 Volts	OK
3.3V MP Voltage	3.3 Volts	OK
3.3V MP Current	2.36 Amps	OK
3.3V MP2 Voltage	3.3 Volts	OK
3.3V MP2 Current	0.18 Amps	OK
DIMM12 Voltage	1.19 Volts	OK
DIMM12 Current	-0.01 Amps	OK
FPGA Core Voltage	0.84 Volts	OK
FPGA Core Current 0	149.53 Amps	OK
FPGA Supply Die Temp	83 degrees C	OK
FPGA Supply Inductor Te..	77 degrees C	OK
FPGA Supply Inductor Te..	77 degrees C	OK
FPGA Slave Supply Temp 0	85 degrees C	OK
FPGA Slave Supply Temp 1	90 degrees C	OK
FPGA Core Temperature	53 degrees C	OK
Board Temperature	46 degrees C	OK
Vcc AUX Voltage	1.76 Volts	OK
Vcc AUX Current	0.72 Amps	OK

Live board power/temperature display is included as part of Toolkit Lite

cooling

Liquid cooling

Air cooling

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Board Specifications

FPGA	• Virtex UltraScale+ VU13P • 48x GTY transceivers at 32.75 Gbps • Up to 3.8 million logic elements • Over 400 Mb of embedded memory • Up to 6 integrated PCIe cores • Up to 11,904 DSP slices with 27x18 multipliers
On-board memory	Flash memory for booting FPGA
Optional DIMM memory	4 DIMM sites, each supporting†: • Up to 128 GBytes DDR4 x72 with ECC • Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)
PCIe interface	x16 Gen1, Gen2, Gen3 interface direct to FPGA (optional; no power used from PCIe connector)
USB ports	• USB C: connects to a breakout board for USB UART, 1 PPS input, 10MHz clock input, UART • Micro USB: connects to USB-JTAG and BMC
UltraPort SlimSAS	• 2 UltraPort SlimSAS on rear edge connected to FPGA via 16x GTY transceivers • Can support an additional x16 or x8 PCIe interface (requires soft IP core and additional slot)
QSFP cages	• 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 transceivers • Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE
Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • I²C bus access • USB 2.0 • Voltage overrides
Cooling	• Liquid-cooled or air-cooled
Size	• ¾-length, standard-height PCIe dual-slot card • 254mm x 111.15mm • Max. component height: 34.79mm dual slot

Development Tools

System development	BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
FPGA development	• FPGA Examples - example Vivado projects • Xilinx Tools - Vivado® Design Suite

XILINX
ALLIANCE PROGRAM
CERTIFIED

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XUPVV4 Ordering Options

XUPVV4 - RW-ABBBBCD-EEFFGGHH-IJK-LMNOP-QRS-T

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)
A	**UltraScale Printed Wiring Board** G = Optimized for VU13P*
BBBB	**FPGA Type and Size** 13VP = Virtex VU13P*
C	**FPGA Core Speed Grade** 1 = Slower 2 = Standard* 3 = Faster
D	**FPGA Temperature Range** E = Extended (Tj = 0 to +100C)*
EE	**DIMM 1‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM L7 = DDR4 128GB LRDIMM Q5 = QDRII+ x18 576 Mb (dual 288Mb)
FF	**DIMM 2‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM L7 = DDR4 128GB LRDIMM Q5 = QDRII+ x18 576 Mb (dual 288Mb)
GG	**DIMM 3‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM L7 = DDR4 128GB LRDIMM Q5 = QDRII+ x18 576 Mb (dual 288Mb)
HH	**DIMM 4‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM L7 = DDR4 128GB LRDIMM Q5 = QDRII+ x18 576 Mb (dual 288Mb)
I	**Oscillator** S = Standard*
J	**Clock Generator A** 0 = 322.265625 MHz*
K	**Clock Generator B** 0 = 322.265625 MHz*
L	**Timing** 0 = None*
M	**QSFP Configuration** 4 = 4 QSFP cages*
N	**SlimSAS** 0 = Installed*
O	**Factory JTAG Header** 0 = Not Installed* 1 = Installed
P	**USB-to-JTAG** 1 = Installed*
Q	**Heatsink** 2 = Passive * L = Liquid cooling
R	**Mechanical Options** 0 = Default* T = Terabox 1400D
S	**Misc. Configuration** 0 = Default
T	**Assembly** 6 = RoHS 6/6

* Default
† Contact Sky Blue or Zerif for availability
‡ DIMM sites 1/2 and sites 3/4 must have the same memory type, or be empty.

International Distributors

Sky Blue Microsystems GmbH
Geisenhausenerstr. 18
81379 Munich, Germany
+49 89 780 2970, info@skyblue.de
www.skyblue.de

In Great Britain:
Zerif Technologies Ltd.
Winnington House, 2 Woodberry Grove
Finchley, London N12 0DR
+44 115 855 7883, info@zerif.co.uk
www.zerif.co.uk