Liquid-Cooled with 300A Power Supply

BittWare a molex company

XUPVVP
PCIe FPGA Board

Power Edition for Monster FPGA Loads

BittWare's XUPVVP is an UltraScale+ VU13P FPGA-based PCIe card, designed for ultra high power applications. The Xilinx UltraScale+ VU13P FPGA gives designers incredible performance potential, with 3.8M logic elements —yet with a power density that makes power and thermal management difficult. The XUPVVP meets this challenge with BittWare's Viper platform, supporting monster FPGA loads, up to 256 GBytes DDR4 or 1152 Mbits QDR-II+, and 4x 100 Gbps Ethernet.

BittWare's Viper platform uses advanced computer flow simulation to drive the physical board design in a thermals first approach, including the use of heat pipes, airflow channels, and arranging components to maximize the limited available airflow in a server. While the default option for the board is air-cooling, the XUPVVP is also available with liquid cooling for rapid heat removal. A 300A FPGA core power supply powers even the largest FPGA loads.

XILINX

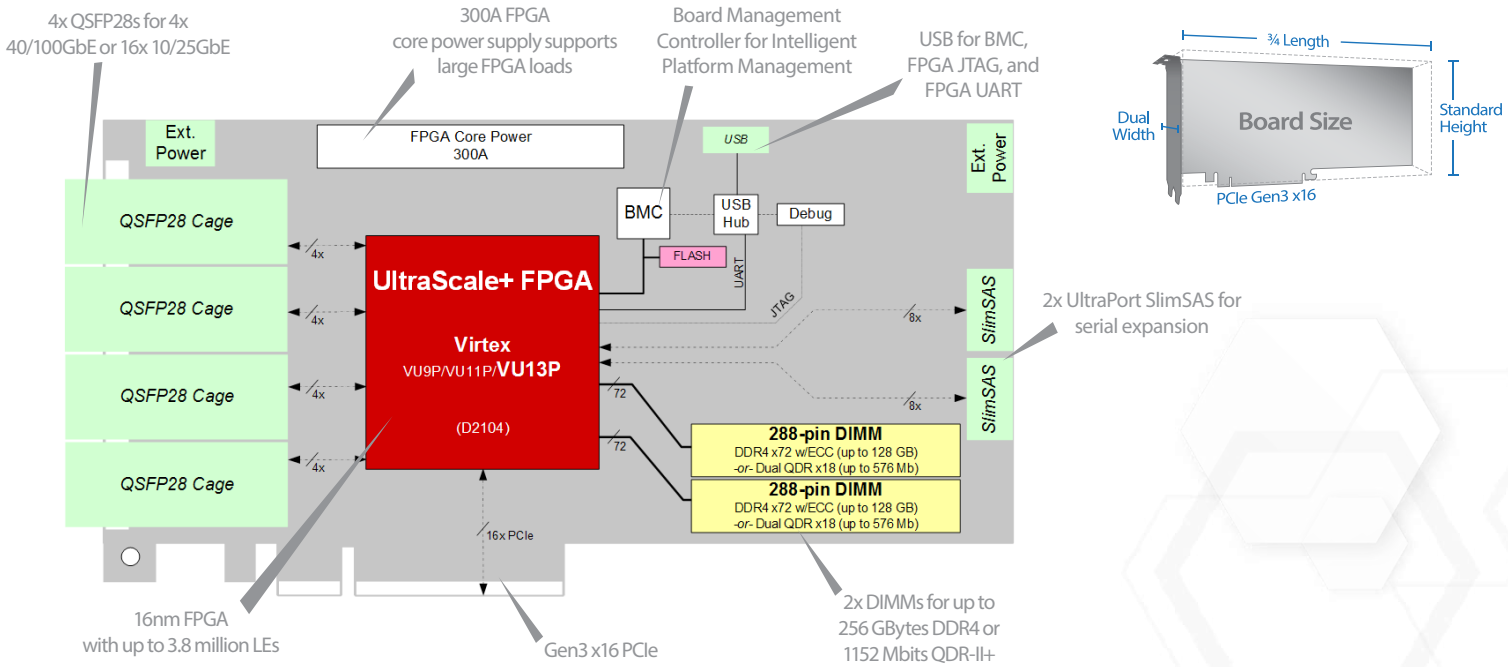
Xilinx VU13P FPGA: lidless package is used by BittWare's Viper thermal management for enhanced cooling performance

key features

300A
FPGA core power supply

Viper platform
Liquid Cooling
option for extreme FPGA loads

Up to VU13P FPGA:
3.8 million LCs
360Mb UltraRAM
FPGA by Xilinx



XUPVVP

PCIe FPGA Board

High-Speed Networking and I/O

The XUPVVP is enabled for high-speed networking with four front panel QSFP+ cages, each supporting 40/100GbE or four 10/25GbE channels. Serial expansion is available through two UltraPort SlimSAS connectors (16x 25Gbps) that can be connected to a second PCIe interface, another XUPVVP, or other devices, including IBM's POWER9 via OpenCAPI. A USB interface is provided for debug and programming support.

System Management

For system management, the XUPVVP is equipped with a Board Management Controller (BMC), which accepts IPMI 2.0 commands. Use it along with BittWare's BittWorks II Toolkit to program the FPGA Flash over USB, monitor board power and temperature, re-program the onboard clocks, and adjust FPGA core voltage. The BMC monitors critical temperatures, voltages, and current and will shut the board down to prevent damage. Recovery from shutdown is also supported, without the need to cycle system power.

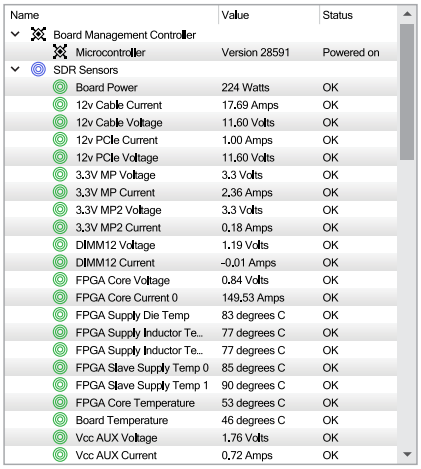
BittWorks II Toolkit

BittWare offers complete software support for the XUPVVP with its BittWorks II software tools. The BittWorks II Toolkit is a suite of development tools that serves as the main interface between the BittWare board and the host system. The Toolkit includes drivers, libraries, utilities, and example projects for accessing, integrating, and developing applications for the BittWare board.

FPGA Examples

BittWare provides FPGA board support IP to simplify integration and development. These example projects illustrate how to move data between the board's different interfaces and are designed to integrate easily with the Xilinx Vivado tools. All examples are available for download on BittWare's developer website.

BWMonitor



Name	Value	Status
Board Management Controller		
Microcontroller	Version 28591	Powered on
SDR Sensors		
Board Power	224 Watts	OK
12v Cable Current	17.69 Amps	OK
12v Cable Voltage	11.60 Volts	OK
12v PCIe Current	1.00 Amps	OK
12v PCIe Voltage	11.60 Volts	OK
3.3V MP Voltage	3.3 Volts	OK
3.3V MP Current	2.36 Amps	OK
3.3V MP2 Voltage	3.3 Volts	OK
3.3V MP2 Current	0.18 Amps	OK
DIMM12 Voltage	1.19 Volts	OK
DIMM12 Current	-0.01 Amps	OK
FPGA Core Voltage	0.84 Volts	OK
FPGA Core Current 0	149.53 Amps	OK
FPGA Supply Die Temp	83 degrees C	OK
FPGA Supply Inductor Te..	77 degrees C	OK
FPGA Supply Inductor Te..	77 degrees C	OK
FPGA Slave Supply Temp 0	85 degrees C	OK
FPGA Slave Supply Temp 1	90 degrees C	OK
FPGA Core Temperature	53 degrees C	OK
Board Temperature	46 degrees C	OK
Vcc AUX Voltage	1.76 Volts	OK
Vcc AUX Current	0.72 Amps	OK

Live board power/temperature display is included as part of Toolkit Lite

XUPVVP

PCIe FPGA Board

Board Specifications

FPGA	• Virtex UltraScale+ VU9P/VU11P/VU13P • 48x GTY transceivers at 32.75 Gbps • Up to 3.8 million logic elements • Over 400 Mb of embedded memory • Up to 6 integrated PCIe cores • Up to 11,904 DSP slices with 27x18 multipliers
On-board memory	Flash memory for booting FPGA
Optional DIMM memory	2 DIMM sites, each supporting†: • Up to 128 GBytes DDR4 x72 with ECC • Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)
PCIe interface	x16 Gen1, Gen2, Gen3 interface direct to FPGA (optional; no power used from PCIe connector)
Utility header	USB, 1 PPS input, 1GbE
UltraPort SlimSAS	• 2 UltraPort SlimSAS on rear edge connected to FPGA via 16x GTY transceivers • Provides 400Gbps board-to-board bandwidth • Can support an additional x16 or x8 PCIe interface (requires soft IP core and additional slot)
QSFP cages	• 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 transceivers • Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE • Provides 400Gbps board-to-board bandwidth
Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • I^2C bus access • USB 2.0 • Voltage overrides
Power & cooling	• Liquid-cooled or air-cooled • Dual external 8-pin power connectors (both must be connected) • 300A FPGA core power supply
Size	• ¾-length, standard-height PCIe dual-slot card • 254mm x 111.15mm • Max. component height: 34.79mm dual slot

Development Tools

System development	BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
FPGA development	• FPGA Examples - example Vivado projects • Xilinx Tools - Vivado® Design Suite

XILINX
ALLIANCE PROGRAM
CERTIFIED

XUPVVP
PCIe FPGA Board

XUPVVP Ordering Options

XUPVVP - RW-ABBBBCD-EEFF-GHI-JKLMN-OPQR-S

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)
A	**UltraScale Printed Wiring Board** G = Optimized for VU13P*
BBBB	**FPGA Type and Size** 13VP = Virtex VU13P*
C	**FPGA Core Speed Grade** 1 = Slower 2 = Standard* 3 = Faster
D	**FPGA Temperature Range** E = Extended (Tj = 0 to +100C)*
EE	**DIMM 1‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM L7 = DDR4 128GB LRDIMM Q5 = QDRII+ x18 576 Mb (dual 288Mb)
FF	**DIMM 2‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM L7 = DDR4 128GB LRDIMM Q5 = QDRII+ x18 576 Mb (dual 288Mb)
G	**Oscillator** S = Standard*
H	**Clock Generator A** 0 = 322.265625 MHz*
I	**Clock Generator B** 0 = 322.265625 MHz*
J	**Timing** 0 = None*
K	**QSFP Configuration** 4 = 4 QSFP cages*
L	**SlimSAS** 0 = Installed*
M	**Factory JTAG Header** 0 = Not Installed* 1 = Installed
N	**USB-to-JTAG** 1 = Installed*
O	**Heatsink** 2 = Passive * L = Liquid cooling
P	**Mechanical Options** 0 = Default*
Q	**eFuse** 0 = None*
R	**Misc. Configuration** 0 = Default
S	**Assembly** 6 = RoHS 6/6

* Default
† Contact BittWare for availability
‡ DIMM sites 1/2 must have the same memory type, or be empty.

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