

XUSP3R

Xilinx UltraScale 3/4-Length PCIe Board with up to VU190, Quad QSFP, and 512 GBytes DDR4

- Xilinx Virtex UltraScale 125/160/190
- Up to four PCIe x8 interfaces supporting Gen1, Gen2, or Gen3
- Four QSFP28 cages for 1x 400GbE, 4x 100GbE, 4x 40GbE, 16x 25GbE, or 16x 10GbE
- **Memory options:**
 - up to 512 GBytes of DDR4 with ECC
 - Up to 288 MBytes QDR-II+
- Board Management Controller for Intelligent Platform Management
- Timestamping support
- Utility I/O: USB 2.0, SATA, serial expansion interface



BittWare's XUSP3R is a 3/4-length PCIe x8 card based on the Xilinx Virtex UltraScale FPGA. The high-performance UltraScale devices provide increased system integration, reduced latency, and high bandwidth for systems demanding massive data flow and packet processing. The board offers extensive memory configurations supporting up to 512 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE. The XUSP3R also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUSP3R ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

Xilinx Virtex UltraScale FPGA

The Xilinx UltraScale FPGAs are built on 20 nm process technology and provide ASIC-like clocking for scalability, performance, and lower dynamic power. The Virtex devices feature two types of multi-gigabit transceivers: 32x 16Gb/s (GTH) and 16x 32.75 Gb/s (GTY). The GTY transceivers enable 400GbE, 100GbE, and 25GbE. The FPGA also supports up to 1,800 DSP slices. The UltraScale FPGAs provide four integrated blocks for PCI Express, supporting x8 Gen3 Endpoint and Root Port designs. Integrated blocks for 150 Gb/s Interlaken and 100 Gb/s Ethernet (100G MAC/PCS) enable simple, reliable support for Nx100G switch and bridge applications.

I/O Interfaces

The XUSP3R provides a variety of interfaces for high-speed serial I/O as well as debug support. Four QSFP28 cages are available on the front panel, each supporting 100GbE, 40GbE, four 25GbE, or four 10GbE channels, for a total of up to 400 Gbps of bandwidth. The four QSFPs can also be combined for 400GbE. The QSFP channels are connected directly to the UltraScale FPGA via 32 Gb/s GTY transceivers. The QSFP cages can optionally be adapted for SFP+.

Two Gen3 x8 PCIe interfaces connect to the FPGA via 16 GTH transceivers, allowing for a x8 PCIe connection in a standard slot or two x8 interfaces in a bifurcated slot. An optional serial expansion interface provides a 16x GTH transceiver port connection to the FPGA and can be used to add serial memory, such as Hybrid Memory Cube (HMC). The expansion site can also be used to connect an additional two x8 PCIe interfaces to the FPGA via a cable assembly connecting to an adjacent board that supports PCIe bifurcation, allowing for a total of four x8 PCIe interfaces.

A USB 2.0 interface is available for debug and programming support, and a SATA connector is available to connect external storage devices or provide direct board-to-board communication. The board also supports timestamping with provision for a 1 PPS and reference clock input.

Memory

The XUSP3R features four DIMM sites that support standard DDR4 DIMMs and proprietary QDR-II+ DIMMs. Each DIMM site supports up to 128 GBytes of DDR4 with optional ECC or up to 72 MBytes QDR-II+ (2 banks x18). Additional on-board memory includes Flash with factory default and support for multiple FPGA images.

XUSP3R

Board Management Controller

The XUSP3R features an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I²C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

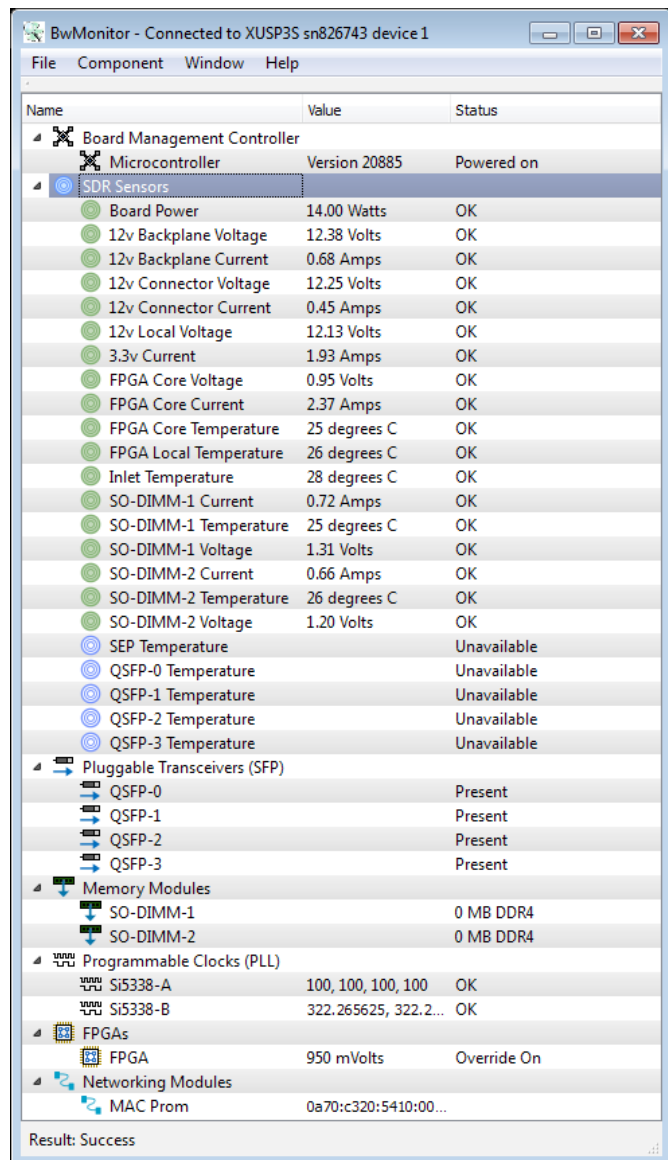
Development Tools

BittWorks II Toolkit

BittWare offers complete software support for the XUSP3R with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Xilinx UltraScale FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

FPGA Example Projects

BittWare offers FPGA example projects to provide board support IP and integration for its Xilinx FPGA-based boards. The example projects easily integrate into existing FPGA development environments and illustrate how to move data between the board's different interfaces. Available example projects include the following: DDR4, QDR-II+, PCIe, 10GbE, LVDS, SerDes, and Double Data Rate I/O.



The screenshot shows the BwMonitor application window titled "BwMonitor - Connected to XUSP3S sn826743 device 1". The window has a menu bar with "File", "Component", "Window", and "Help". Below the menu bar is a table with three columns: "Name", "Value", and "Status". The table is organized into a tree structure with expandable/collapsible icons. The "Board Management Controller" is expanded, showing a "Microcontroller" (Version 20885, Powered on) and "SDR Sensors". The "SDR Sensors" section lists various sensors with their values and status (OK or Unavailable). Other sections include "Pluggable Transceivers (SFP)", "Memory Modules", "Programmable Clocks (PLL)", "FPGAs", and "Networking Modules".

Name	Value	Status
Board Management Controller		
Microcontroller	Version 20885	Powered on
SDR Sensors		
Board Power	14.00 Watts	OK
12v Backplane Voltage	12.38 Volts	OK
12v Backplane Current	0.68 Amps	OK
12v Connector Voltage	12.25 Volts	OK
12v Connector Current	0.45 Amps	OK
12v Local Voltage	12.13 Volts	OK
3.3v Current	1.93 Amps	OK
FPGA Core Voltage	0.95 Volts	OK
FPGA Core Current	2.37 Amps	OK
FPGA Core Temperature	25 degrees C	OK
FPGA Local Temperature	26 degrees C	OK
Inlet Temperature	28 degrees C	OK
SO-DIMM-1 Current	0.72 Amps	OK
SO-DIMM-1 Temperature	25 degrees C	OK
SO-DIMM-1 Voltage	1.31 Volts	OK
SO-DIMM-2 Current	0.66 Amps	OK
SO-DIMM-2 Temperature	26 degrees C	OK
SO-DIMM-2 Voltage	1.20 Volts	OK
SEP Temperature		Unavailable
QSFP-0 Temperature		Unavailable
QSFP-1 Temperature		Unavailable
QSFP-2 Temperature		Unavailable
QSFP-3 Temperature		Unavailable
Pluggable Transceivers (SFP)		
QSFP-0		Present
QSFP-1		Present
QSFP-2		Present
QSFP-3		Present
Memory Modules		
SO-DIMM-1		0 MB DDR4
SO-DIMM-2		0 MB DDR4
Programmable Clocks (PLL)		
Si5338-A	100, 100, 100, 100	OK
Si5338-B	322.265625, 322.2...	OK
FPGAs		
FPGA	950 mVolts	Override On
Networking Modules		
MAC Prom	0a70:c320:5410:00...	

Result: Success

BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

Specifications

BOARD SPECIFICATIONS

FPGA

- Xilinx UltraScale FPGA
 - Virtex UltraScale125/160/190
- Multi-gigabit transceivers
 - 16x GTY at 32.75 Gbps and 32x GTH at 16 Gbps
- Up to 1.9 million logic elements
- Up to 132 Mb of embedded memory
- Up to 4 integrated PCIe cores
- Up to 1,800 DSP slices with 27x18 multipliers

On-Board Memory

- Flash memory for booting FPGA

Optional DIMM Memory

- 4 DIMM sites, each supporting*:
 - Up to 128 GBytes DDR4 x72 with ECC
 - Up to 576 Mbits QDR-II x18

PCIe Interface

- Two x8 Gen1, Gen2, Gen3 interfaces direct to FPGA (One x8 interface in a standard slot; two x8 interfaces requires bifurcated slot)
- Serial Expansion Port can be used for two additional x8 interfaces

USB Header

- Micro USB port (USB 2.0) for debug and programming FPGA and Flash

QSFP Cages

- 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 GTY transceivers
- Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

Serial Expansion Port

- Expansion interface to FPGA via 16x GTH transceivers (optional; requires second slot)

Serial ATA

- SATA connector, connected to FPGA

Timestamping

- 1 PPS input
- Reference clock input

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- 3/4-length, standard-height PCIe dual slot card
- 241mm x 111.15mm
- Max. component height: 34.79mm dual slot

DEVELOPMENT TOOLS

System Development

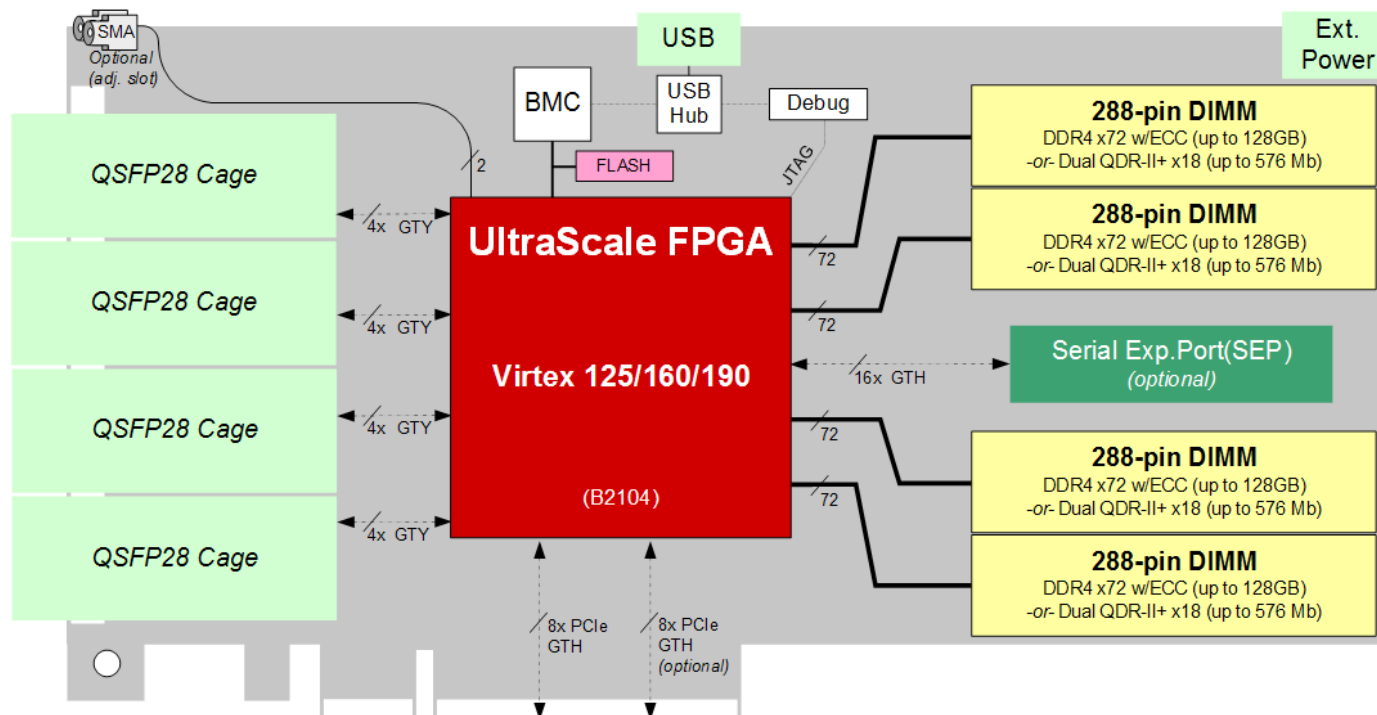
- [BittWorks II Toolkit](#) - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

FPGA Development

- [FPGA Example Projects](#)
 - PCIe Gen3x8 Base Project
 - DDR4
 - QDR II/II+
 - SerDes (iBERT)
- [Xilinx Tools](#)
 - Vivado® Design Suite
 - USB to JTAG converter

*DIMM sites 1 & 2 and DIMM sites 3 & 4 must have the same memory types, since they share voltage settings. For example, if DIMM 1 is DDR4, then DIMM 2 must be as well (or be empty).

Figure 2: XUSP3R System Block Diagram



XUSP3R Ordering Options

XUSP3R - RW-ABBBBCD-EEFFGGHH-IJKLMNOP-QR-S-T					
RW	Ruggedization 0U = Commercial (0°C to 50°C)*	GG	DIMM 3‡ 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = Dual QDRII+ x18 144Mb Q5 = Dual QDRII+ x18 288Mb	M	Serial Expansion Port 0 = Not Installed 1 = Installed*
A	UltraScale Printed Wiring Board D = Optimized for VU190 FPGA*			N	Factory JTAG Header 0 = Not Installed* 1 = Installed
BBBB	FPGA Type and Size 190V = Virtex VU190*			O	USB-to-JTAG 0 = Not Installed 1 = Installed*
C	FPGA Core Speed Grade 1 = Slower 2 = Standard* 3 = Faster	HH	DIMM 4‡ 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = Dual QDRII+ x18 144Mb Q5 = Dual QDRII+ x18 288Mb	P	Heatsink 3 = Active 2-slot* 4 = Passive 2-slot
D	FPGA Temperature Range E = Extended (Tj = 0 to +100C)*			Q	Misc. Configuration 0 = Default
EE	DIMM 1‡ 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = Dual QDRII+ x18 144Mb Q5 = Dual QDRII+ x18 288Mb			I	Oscillator S = Standard
FF	DIMM 2‡ 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = Dual QDRII+ x18 144Mb Q5 = Dual QDRII+ x18 288Mb	J	Auxiliary Oscillator 0 = 322.265625*	R	Power Supply R = Right angle connector* V = Vertical connector
		K	Timing S = Front panel SMAs (in adj. slot) X = On-board circuits only*	S	Mechanical Options 0 = No stiffener S = Standard stiffeners*
		L	QSFP Configuration 4 = 4 QSFP cages	T	Assembly 6 = RoHS 6/6

* Default

‡ DIMM sites 1/2 and sites 3/4 must have the same memory type, or be empty.

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