

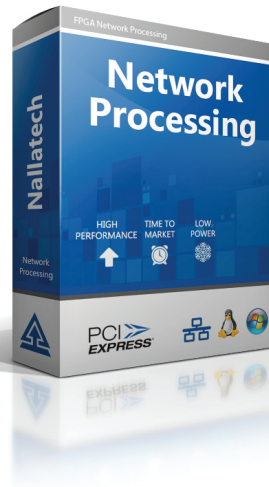
PCIe-180

FPGA Network Processing Card

The PCIe-180™ low profile network processing card provides a powerful PCI Express computing and I/O platform for FPGA development and deployment across a range of application areas including Signal Intelligence, Network Security and Algorithm Acceleration.

The PCIe-180 features an XFP module supporting 10Gb Ethernet and OC192 SONET via PCI backplate. This network interface is directly coupled to a Xilinx FPGA and a flexible, high bandwidth configuration of SRAM and SDRAM memory.

The PCIe-180 is compatible with most high density server and blade platforms from leading vendors.



XILINX
ALL PROGRAMMABLE™



Low profile 10GbE Accelerator Card Featuring a Xilinx FPGA and Random Access Memory

Key features

- Low profile PCI Express form factor
- XFP supporting 10GbE and OC192 SONET
- 8-lane PCI Express Gen 1 host interface
 - Up to 1.1 GB/s WRITE (system-to-card)
 - Up to 1.3 GB/s READ
- Xilinx Virtex-5 LX155-1 user FPGA
- Five independent banks of DDR-II SRAM memory
- Single bank of DDR2 SDRAM memory
- Linux and Windows 7 Operating System support

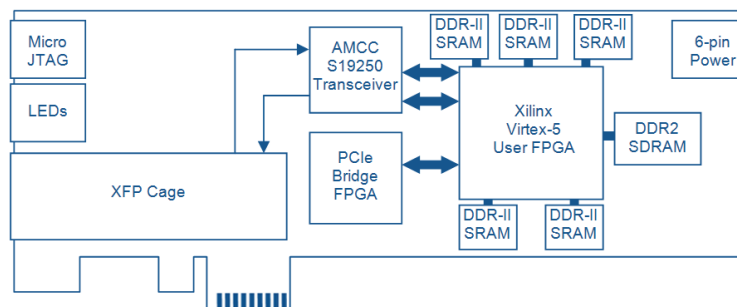
Benefits

- » **Commercial-off-the-shelf (COTS) hardware**
Shorten time to market and reduce risk
- » **PCI Express**
Industry standard interconnect
- » **8-lane**
Ubiquitous high performance host interface
- » **Comprehensive suite of IP**
Invest time developing your algorithm, not interfaces

The Leader in FPGA
Accelerated Computing

Nallatech
a **molex** company

Functional diagram



Full specification

Form factor	Host interface	Electrical	Cooling
<ul style="list-style-type: none"> Low profile, single width PCI Express card Half height, half length 2.713 x 6.6 inches 	<ul style="list-style-type: none"> 8-lane PCI-Express 1.1 Up to 2.4GB/s total Host bandwidth Actual performance is host computer chipset and operating system dependant PCIe host interface IP core included 	<ul style="list-style-type: none"> On-card power derived from 3.3V and 12V PCIe slot FPGA power dissipation is application dependent 6-pin GPU-style header for applications that need more power. Please contact Nallatech for further information 	<ul style="list-style-type: none"> Available with either active (chipfan) or passive (heatsink) cooling Passive heatsink option requires forced-air cooling Please contact Nallatech for further information
Processing	PCI backplate interfaces	Quality	Environmental
<ul style="list-style-type: none"> Xilinx Virtex-5 LX155-1 user FPGA Please contact Nallatech for other supported FPGAs options 	<ul style="list-style-type: none"> XFP cage <ul style="list-style-type: none"> AMCC- S19250 physical layer bridge chip supports 10GbE and OC192 SONET Converts between 10Gbps XFP interface and two 16-bit LVDS FPGA interfaces operating at 622.08Mbps (10GbE) and 644.53Mbps (SONET) AMCC interface IP core included Tri-color LEDs and uJTAG header 	<ul style="list-style-type: none"> Manufactured to IPC610-Class 2 standard. Designed and Supplied to ISO9001:2000 certification ROHS compliant 	<ul style="list-style-type: none"> Cooling: Air convection Operating temperature: 0°C to 50°C Storage temperature: -20°C to 80°C Relative humidity: 45 to 95% (non-condensing)
SRAM memory	Application Programming Interface (API)	Deliverables	Ordering
<ul style="list-style-type: none"> 40 MB DDR-II SRAM Five independent 8 MB banks 32-bit data bus per bank ECC and Parity support Operating frequency: 250 MHz Max. bandwidth per bank: 2 GB/s Max. total bandwidth: 10 GB/s DDR-II SRAM controller IP core included 	<ul style="list-style-type: none"> NallaLIB API for 64-bit Linux Runtime FPGA programming, hardware control, and application communication 	<ul style="list-style-type: none"> PCIe-180 FPGA card Micro JTAG adapter Full and half height PCI backplates Product DVD NallaLIB API and documentation IP cores (including VHDL source) 30 days product maintenance (technical support, support lounge access) 	<ul style="list-style-type: none"> Contact us for leadtime and pricing information
SDRAM memory	Application development software		
<ul style="list-style-type: none"> 512 MB DDR2 SDRAM 72-bit data bus ECC and Parity support Operating frequency: 250MHz Max. total bandwidth: 4 GB/s Auto refresh capable DDR2 SDRAM controller IP core included 	<ul style="list-style-type: none"> Supports multiple design flows including VHDL and Verilog Compatible with Xilinx ISE and all major synthesis design flows 		

International Distributors



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