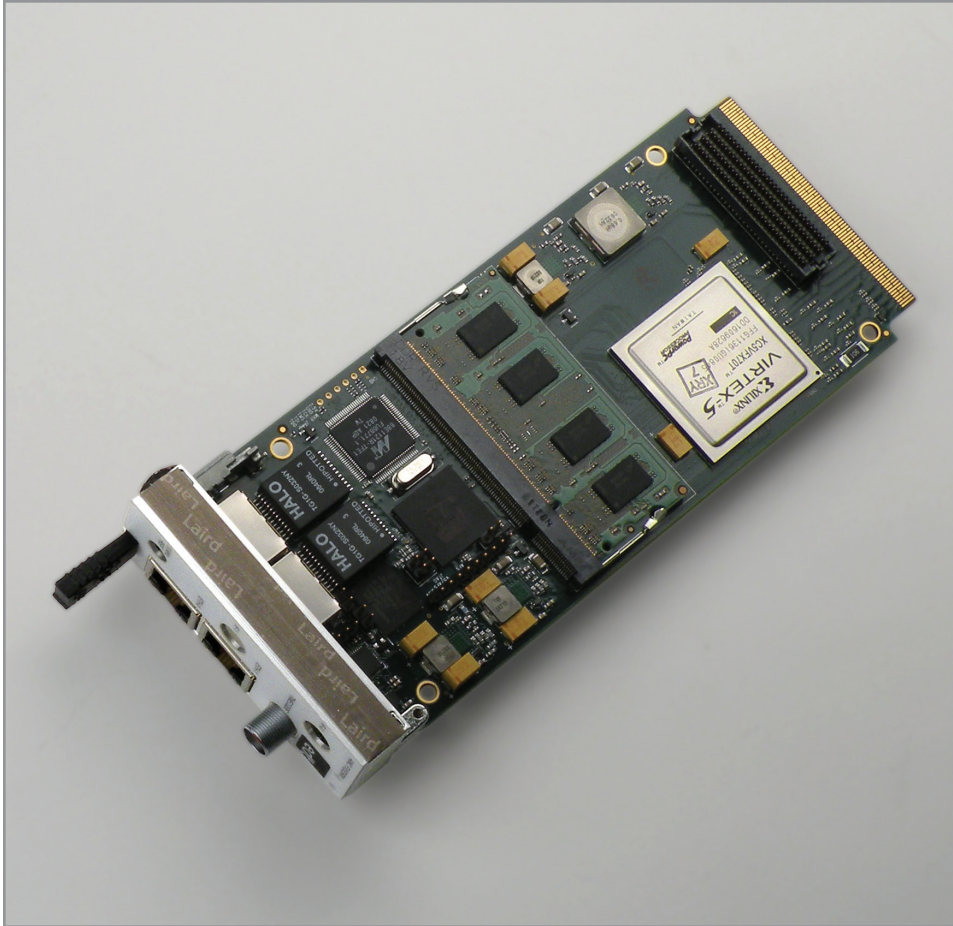


AMC FX5

AMC main board with Virtex 5 FXT FPGA



Description

The AMC FX5 is a main board for AMC MicroTCA or ATCA that provides powerful DMA, memory, and other resources to a mezzanine board. It supports 1GbE, PCIe, or 10GbE.

Two front-panel ports support 1000 BASE-T, and two AMC ports (0 and 1) support 1000 BASE-X. AMC ports 4-11 (the fat pipes region) can support either PCI Express or ethernet.

Signals connected to the mezzanine board include 44 LVCMOS (2.5v) single-ended; 40 LVDS pairs; and 4 full-duplex RocketIO channels.

In addition, the board has 1 GB DRAM (DDR2 SODIMM); a crystal oscillator (XCO), user-programmable from 10 to 215 MHz; and a Xilinx Virtex 5 FPGA (XC5VFX70T or optional 100T) with PowerPC 440 CPU. Programmable FPGA resources are provided through the mezzanine board.

A time code input (1 pps or IRIG-B) also is provided.

EDT provides FPGA configuration files. Custom configuration files can be requested.

Features

Main board (AMC uTCA / ATCA) - provides DMA, memory, and other resources to a mezzanine board, which provides programmable FPGA resources

Interfaces:

- Front panel = two 1000 BASE-T
- AMC connector = two 1000 BASE-X, plus fat pipes region (configurable for PCIe or ethernet)

Signals connected to mezzanine board:

- 44 LVCMOS (2.5v) single-ended signals
- 40 LVDS signal pairs
- 4 full-duplex RocketIO channels

DRAM: 1 GB DDR2 SODIMM

XCO: One user-programmable (10-215 MHz)

Time code: 1 pps, IRIG-B, or other input

Applications

EDT mezzanine board support for UTCA / ATCA form factors

Specifications

| | | |
|---------------------|--|--|
| Product Type | AMC main board for uTCA or ATCA; it supplies DMA, memory, and other resources to a mezzanine board. | |
| FPGA Resources | One non-programmable Xilinx Virtex 5 FXT FPGA (XC5VFX70T or optional 100T) with PowerPC 440 CPU. Programmable FPGA resources are available on the corresponding mezzanine board. | |
| Memory | DRAM (200-pin SODIMM DDR2) | 1 GB |
| Clocks | One programmable XCO | 10-215 MHz |
| Data Rates | Dependent on such factors as data format, mezzanine board, and system variables: | |
| | 1GbE | 200 MB/s |
| | PCI Express | 700 MB/s |
| | 10GbE | TBD |
| Data Format (I/O) | Time code (from external receiver) | 1 pps, IRIG-B, or other input, with user-configurable output |
| | Other data (depending on mezzanine board used) | 1 GbE (front and back) or PCIe (back) or 10GbE |
| Compliance | PICMG AMC.0 R2.0 | |
| Connectors | One 7-pin Lemo for time code Two RJ45 One 6-pin .100" x 1 row square .025" Two 2-pin .100" x 1 row square .025" One SEAF connector to mezzanine board | 1 pps, IRIG-B, or other input, with user-configurable output 1000 BASE-T For FPGA JTAG (IEEE 1149.1) For RS232 UART Mate to SAMTEC SEAM-30-11.0-S-08-2-A: - 44 LVCMOS (2.5v) single-ended signals - 40 LVDS signal pairs - 4 full-duplex RocketIOm channels |
| Cabling | Consult EDT for purchase options. | |
| Physical | This single-width main board pairs with a mezzanine board, so total weight and height are dependent on the mezzanine board used. | |
| | Weight | With mezzanine board: 8.6 oz. |
| | Dimensions | With mezzanine board: 7.25 x 2.875 x 1.25 in. |
| Environmental | Temperature (operating / non-operating) | 0° to 40° C / -40° to 70° C |
| | Humidity (operating / non-operating) | 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C |
| System and Software | System must have a PCI Express bus (1 or 4 lanes). Software is included for Windows and Linux; for versions, see www.edt.com . | |

Ordering Options

- Mezzanine board: DRX or OCM2.7G
- Data format: 1GbE / PCIe / 10GbE (dependent on mezzanine board)
- FPGA: XC5VFX**70T** / 100T

Bold is default. For more options, see mezzanine board detail. **Ask** about custom options.

Contact



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