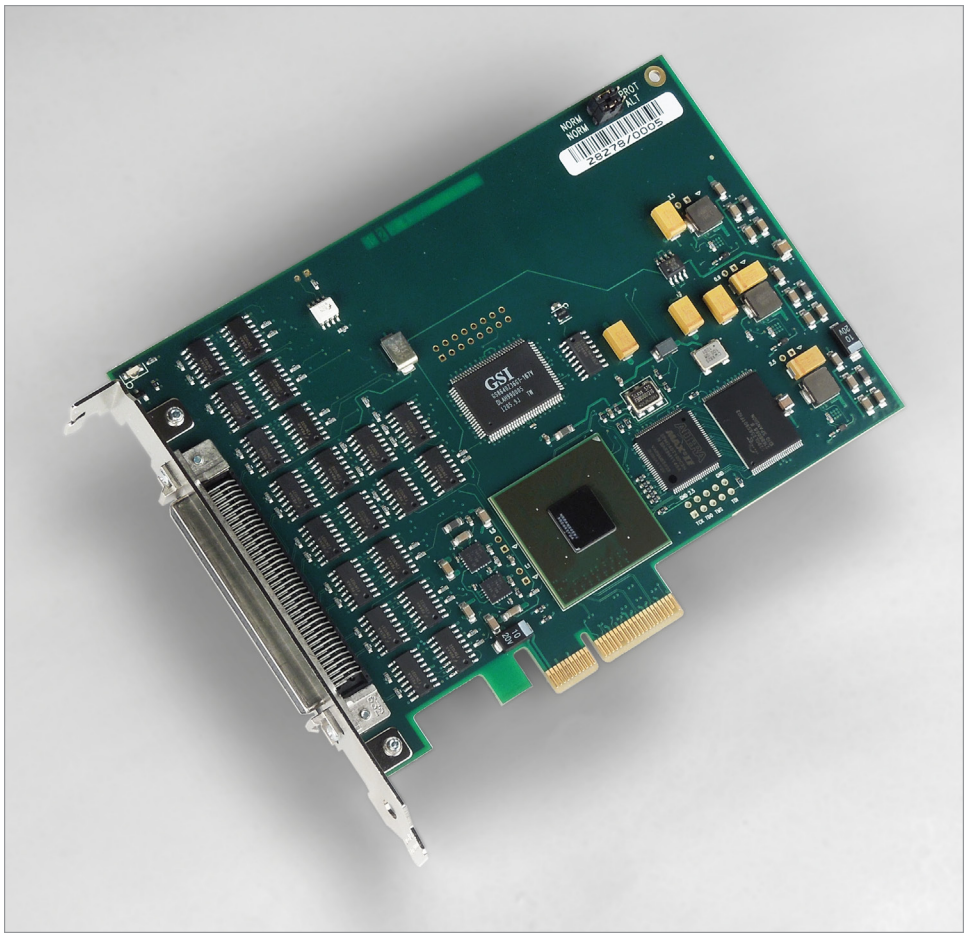
edt
a HEICO company

PCIe4 CDa

PCI Express 4-lane interface for configurable DMA and synchronous I/O



Features

- PCIe x4 interface for high-speed DMA and synchronous LVDS or RS422 I/O
- FPGA: One user-configurable Altera Arria II
- Buffers: Integrated FIFOs for input and output
- DMA channels:
  - Standard = one 16- or 32-bit parallel, or sixteen synchronous serial
  - Low-latency = one 16-bit parallel
- I/O: LVDS or RS422
- I/O data rates (150 Mb/s):
  - 1 parallel channel = 600 MB/s total for 32-bit, or 300 MB/s total for 16-bit
  - 1 serial channel = 150 Mb/s
- Hardware protocol: Synchronous (each signal has its own sample clock)
- VHDL: User-accessible in the FPGA

Description

The PCIe4 CDa is a PCI Express 4-lane interface that enables fast DMA and synchronous I/O to transfer differential (LVDS or RS422) data between an external device and a host computer.

The board provides one Altera Arria II GX FPGA (EP2AGX450D) which combines PCIe functionality (for DMA) and UI functionality (for I/O). The buffers are integrated FIFOs for input and output. The FPGA configuration options are...

- Standard DMA: One 16- or 32-bit parallel channel, or sixteen synchronous serial channels; or
- Optional low-latency DMA: One 16-bit parallel channel.

Observed data rates on the PCIe connector are up to 700 MBytes per second. Observed data rates on the I/O connector are 150 Mbits per second:

- 1 parallel channel = 600 MB/s total for 32-bit, or 300 MB/s total for 16-bit
- 1 serial channel = 150 Mb/s

The hardware protocol is synchronous: all data and control signals are sampled by a clock transmitted along with them. This sample clock can be generated by the DMA interface, the user device, or both.

For custom designs, EDT allows access to the source VHDL in the FPGA.

Applications

- Simulation
- Imaging devices
- Scanners
- Plotters
- Device control
- General-purpose data acquisition

Specifications

Product Type	PCIe4 CDa is a PCIe 4x interface that provides high-speed DMA and synchronous I/O for LVDS or RS422.	
FPGA Resources	One Altera Arria II GX (EP2AGX450D)	This single FPGA combines PCIe and UI functionalities.
Other Resources	Buffers	Integrated FIFOs for input and output
Memory	SRAM	0 or optional 8 MB
Clock	1 PLL clock generator 1 Si570 clock generator	Programmable from 168 Hz to 100 MHz Programmable from 10 to 800 MHz
Data Rates	150 Mbits per second	1 parallel channel = 600 MB/s total for 32-bit, or 300 MB/s total for 16-bit 1 serial channel = 150 Mb/s
Data Format (I/O)	LVDS or RS422	
PCI Express Compliance	PCIe version DMA Number of lanes	PCIe 1.1 One channel or sixteen channels 4
Connectors	I/O: One AMP 787190-8 high-density 80-pin (mates with AMP 749621-8, backshell 749196-2)	
Physical	Weight Dimensions (with backplane)	3.6 oz. typical 6.5 x 3.8 x 0.5 in.
Environmental	Temperature Humidity	Operating: 10° to 40° C Non-operating: -40° to 70° C Operating: 1% to 90%, non-condensing at 40° C Non-operating: 95%, non-condensing at 40° C
System and Software	System must have a PCIe 1.1 bus (4 or more lanes) which is not dedicated to display use only. Software is included for Windows, Linux, and Mac OS X; for versions, see our website.	

Ordering Options

- Memory: **0** / 8 MB
- I/O: LVDS / RS422
- DMA: **One-** / multi-channel

Bold is default. **Ask** about custom options.

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