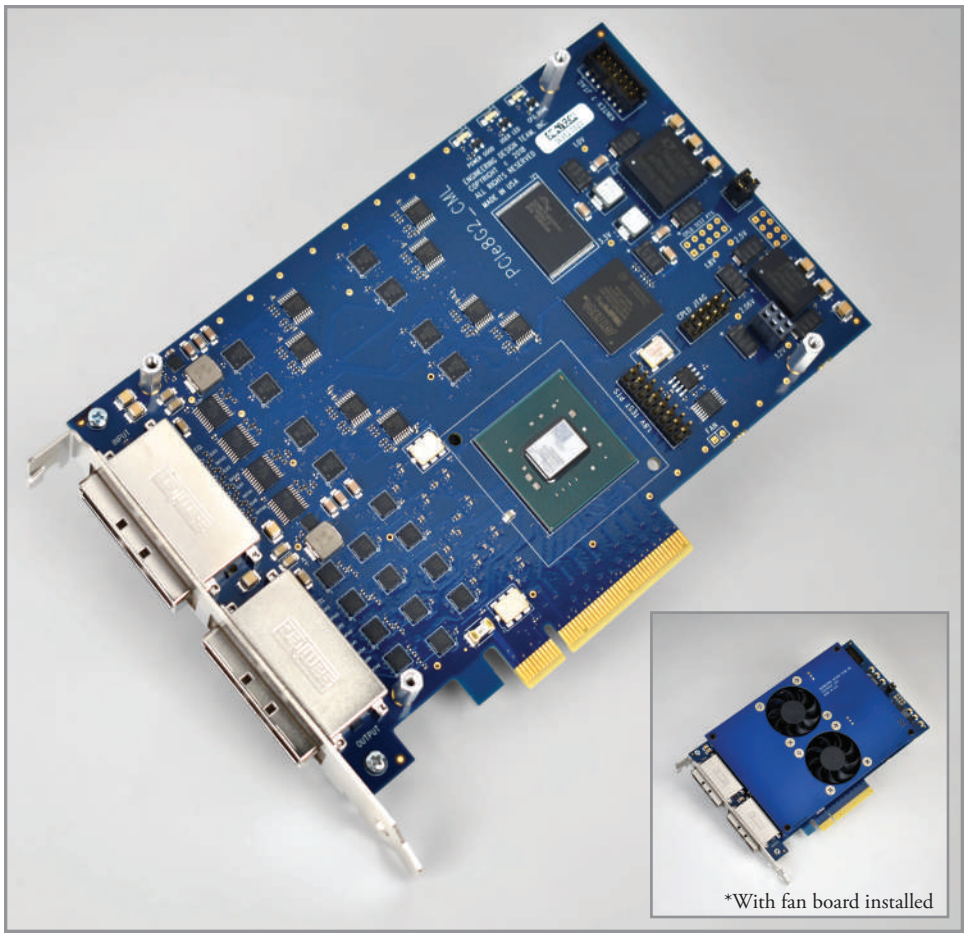
PCIe8 CML-ECL

PCIe 8-lane interface for configurable DMA of 4 CML and 4 ECL I/O channels



*With fan board installed

Features

- PCIe x8 interface for high-speed DMA and synchronous CML and ECL I/O
- One user-configurable Xilinx Kintex 7 FPGA
- Integrated FIFOs for input and output
- 16 DMA channels, 8 for receive, 8 for transmit
- I/O (standard): 4 CML input/output channels and 4 ECL input/output channels
- CML I/O data rates of up to 1300 Mb/s per channel
- ECL I/O data rates of up to 1400 Mb/s per channel
- Synchronous hardware protocol (each channel has its own independent clock)
- User-accessible VHDL in the FPGA

Description

The PCIe8 CML-ECL is a PCI Express 8-lane interface that enables fast DMA and synchronous I/O to transfer CML and ECL data between an external device and a host computer. 8 bidirectional channels are supported; four CML and four ECL.

The board provides one Xilinx Kintex 7 FPGA (XC7K160T) which combines PCIe functionality (for DMA) and UI functionality (for I/O). The buffers are integrated FIFOs for input and output.

Observed data rates on the I/O connector are up to 1300 Mbits per second for the CML channels and up to 1400Mbits per second on the ECL channels.

The hardware protocol is synchronous: all data and control signals are sampled by a clock transmitted along with them. This sample clock can be generated by the DMA interface, the user device, or both.

EDT provides FPGA configuration files supporting standard operations. Custom configuration files can be requested.

Applications

- Signal receiver and transmitter
- Communications monitoring (serial data)
- General-purpose data acquisition

Specifications

Data Format (I/O)	**Standard**	**ECL**	**CML**
	Independent I/O channels	4	4
	Termination (differential)	50 ohms to -2 V DC	100 ohms line to line
	Output jitter compliance	Yes	Yes
	Output independent Clock/Data Delay Control	Yes	Yes
Data Rates	CML	Up to 1.3GHz (162.5 MB/s)	
	ECL	Up to 1.4GHz (175 MB/s)	
Clocks	2 Si570 clock generators: Programmable from 10 to 800 MHz (1 for the ECL channels and 1 for the CML channels)		
FPGA Resources	One Xilinx Kintex 7 (XC7K160T): This single FPGA combines PCIe and UI functionalities.		
PCI Express Compliance	PCIe version	3.0	
	Number of DMA channels	16	
	Number of lanes	8	
Connectors	I/O: Two SAMTEC ERI8-031-S-D-RA 62-pin (mates with SAMTEC cable EPLSP-031-1000)		
Physical	Weight	6.4 oz. typical with breeze cooling board	
	Dimensions (with Breeze Cooling Board)	6.5 x 4.4 x 0.75 in.	
Environmental	Temperature	Operating: 10° to 40° C	
		Non-operating: -40° to 70° C	
	Humidity	Operating: 1% to 90%, non-condensing at 40° C	
		Non-operating: 95%, non-condensing at 40° C	
System and Software	System must have a full-height PCIe 1.1, 2.0 or 3.0 (recommended) slot x4 or greater, not dedicated to display use only. Software & drivers are included for Windows and Linux; for versions, see edt.com.		

International Distributors

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