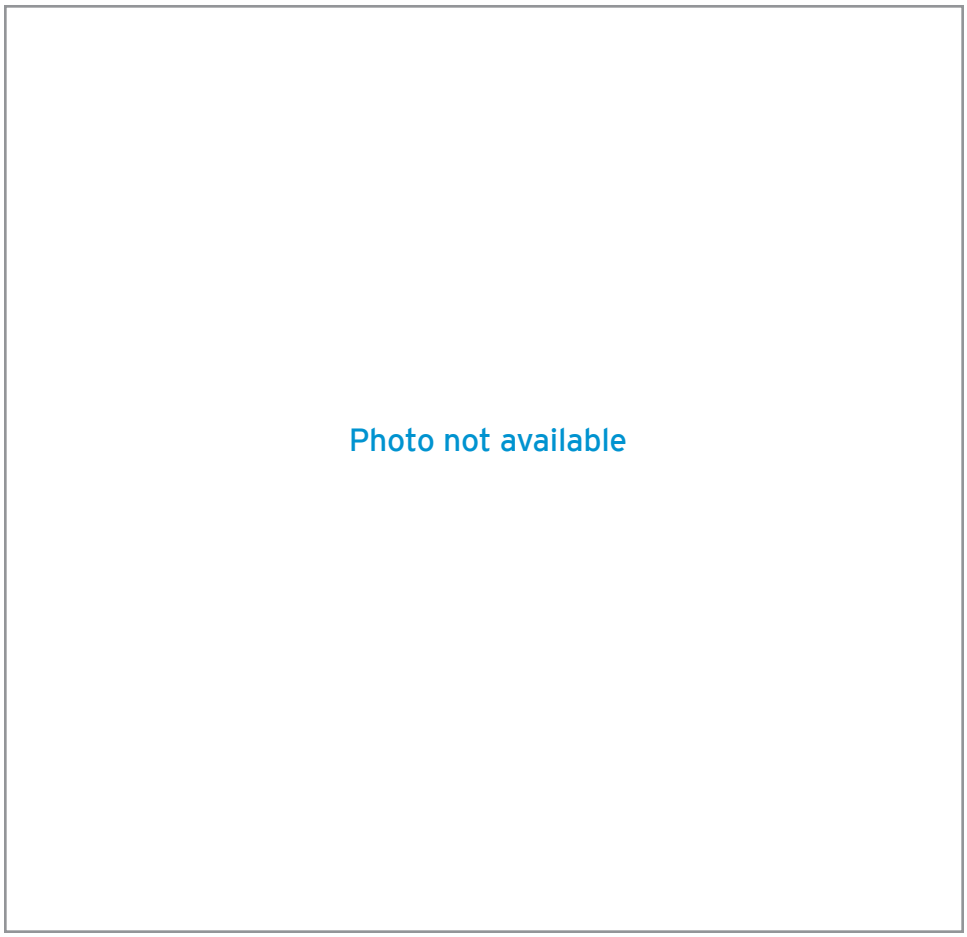
PCIe8g3 A5-40G

PCIe Gen3 x8 board with Arria V FPGA and 40G QSFP+



Description

The PCIe8g3 A5-40G is a fast, versatile low-profile PCI Express (PCIe, Gen3) x8 interface, available with either a full or a half-height back panel. It has one 40G QSFP+ port and supports 40GbE or OTU3.

The port, which has its own reference clock programmable for 1–808 MHz., links to the FPGA for serialization / deserialization (SERDES) and clock recovery.

The single FPGA is an Altera Arria V GZ (E3, E5, or E7) with access to one 64-bit wide 2 GB block of DRAM (DDR3), which can act as a data buffer. The FPGA provides up to 8 independent DMA channels via EDT FPGA configuration files.

A time code input (1 pps or IRIG-B) also is included, with an option for either DB9 or BNC cabling.

EDT FPGA configuration files are included to support 40GbE (at the PCS and PMA layers) and OTU3 (raw, framed, framed and descrambled). Custom files can be requested.

Features

- PCIe (Gen3) x8 half-height interface (full- or half-height back panel) with one 40G QSFP+
- Data formats: 40GbE, OTU3
- FPGA + DMA: One user-programmable Altera Arria V 5AGZ (E3, E5, or E7), configurable for up to 8 independent DMA channels
- DRAM (DDR3): One 64-bit wide block of 2 GB
- EDT intellectual property for 40GbE PCS and PMA layers, and G.709 framing
- Time code input: 1 pps or IRIG-B, with user-configurable output

Applications

- Telecommunications monitoring, recording, and processing
- SONET/SDH to ethernet conversion
- Multiple other network processing applications

Specifications

Product Type	PCIeGen3 x8 board with Altera Arria V FPGA and one 40G QSFP+ for 40GbE or OTU3.
FPGA Resources + DMA	One programmable FPGA (Altera Arria V GZ (E3, E5, or E7), user-configurable for up to 8 independent DMA channels
Memory	DRAM (DDR3), one 64-bit wide 2 GB block for snapshot recording / data buffering
Clocks (Reference)	The port has one reference clock (programmable from 1 to 808 MHz), plus support for reference loop timing.
Data Rates	Dependent on such factors as data format and system variables.
Data Format (I/O)	The board supports 40GbE or OTU3, as shown below. Also provided is a time code input (to connect to an external source) for 1 pps, IRIG-B, or other input, with user-configurable output.
Transcievers	The board has multiple transceiver options, as shown below.

Up to one QSFP+	**ELECTRICAL**	**OPTICAL (40GbE) QSFP+ 850 nm**
Output power (dBm)	–	-7.6 to -1.0
Center wavelength (nm)	–	840–860
Sensitivity (dBm)	–	-5.4
Max. input power (dBm)	–	+3.4
Connector	–	1x12 MPO

Cooling	Active heat sink	
Connectors	One 7-pin Lemo for time code input One MPO on QSFP+	
Cabling	To 7-pin Lemo on board, from time code source For other cabling, consult EDT for purchase options.	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)
Physical	Weight Dimensions	4.0 oz. (typical, with active heat sink but without transceivers) 6.6 x 2.7 x 0.75"
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	System must have a PCI Express bus (8 or 16 lanes) that is not dedicated to display use only. Software is included for Windows and Linux; for versions, see www.edt.com.	

Ordering Options

- Full- or half-height backpanel
- FPGA: E3 / E5 / E7
- Transceivers: [options above]
- Cabling (for time code input): DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.

International Distributors

sky blue microsystems

Sky Blue Microsystems GmbH
Geisenhausenerstr. 18
81379 Munich, Germany
+49 89 780 2970, info@skyblue.de
www.skyblue.de

ZERIF TECHNOLOGIES LTD.
A SKY BLUE COMPANY, FOUNDED 1999

In Great Britain:
Zerif Technologies Ltd.
Winnington House, 2 Woodberry Grove
Finchley, London N12 0DR
+44 115 855 7883, info@zerif.co.uk
www.zerif.co.uk