edt
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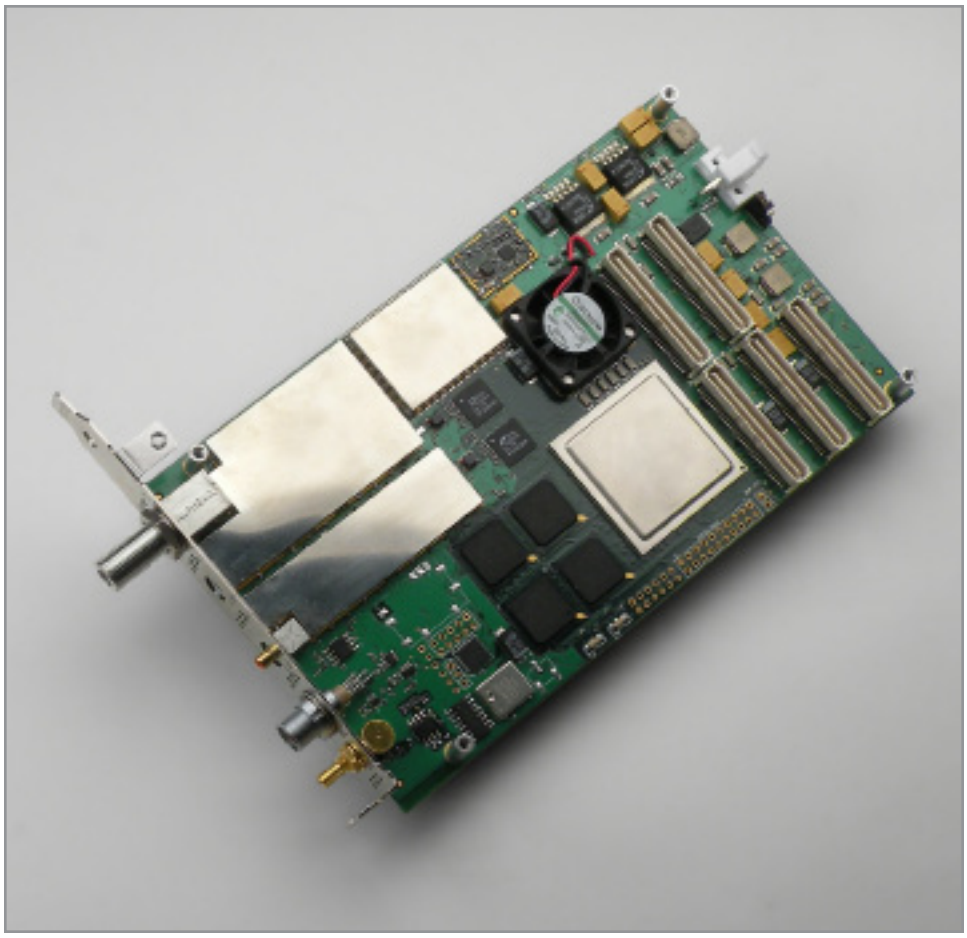
SRXL2

Signal receiver and processor for IF and L-band, v. 2



Features

- Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory
- Two configurable RF ports (0 and 1) with simultaneous 12-bit ADC
- Port 0 – supports IF direct module (IDM) or IF mixer module (IMM):
  - IDM supports input over 10 MHz, with optional 90-MHz lowpass filter
  - IMM supports input of 140 or 160 MHz, mixed to center frequency of 55 MHz; bandwidth is determined by external filtering (not provided)
- Port 1 – supports either module above, or L-band module (LBM) for input of 900 to 2250 MHz, mixed to center frequency of 187.5 MHz, with 1 MHz tuning resolution; bandwidth is 104 MHz
- FPGA: One programmable Xilinx Virtex 4 SX XC4VSX55
- Graychips: Four (TI GC4016) for a total of 16 DDCs
- Sample clock: Programmable to any frequency from 10 to 250 MHz
- Timebase: 10 MHz TCXO or user input
- Time code input: 1 pps or IRIG-B, with user-configurable output

Description

The SRXL2 is a mezzanine board that pairs with a PCI / PCIe main board to process two simultaneous RF inputs.

Sampling rates depend upon the module used: IF direct module (IDM), IF mixer module (IMM), or L-band module (LBM). Port 0 supports either of the first two, while port 1 supports any of the three modules.

IDM supports any frequency over 10 MHz that meets Nyquist criteria. A 90-MHz lowpass filter is optional.

IMM supports 140 or 160 MHz input, mixed to 55 MHz (center). Bandpass filtering, not provided, is performed externally.

LBM supports 900 to 2250 MHz input, mixed to 187.5 MHz (center) with 1MHz tuning resolution; bandwidth is 104 MHz.

Module outputs are digitized with 12-bit precision ADCs and captured in the programmable Xilinx Virtex 4 SX FPGA. The FPGA can perform signal processing or serve as a configurable switch matrix to route data to the main board and four Graychips (GC4016), each with four digital down-converters (DDCs) for a total of sixteen DDCs.

For the timebase, you can use the 10 MHz TCXO provided, or connect your own source via the reference input. A time code input (1 pps or IRIG-B) also is included.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Applications

- Satellite receiver
- Software-defined radio
- Surveillance / spectrum monitoring
- Digital tuning
- Test and measurement equipment

Specifications

Product Type	Signal receiver interface (v. 2) for IF and L-band; it requires an EDT PCI / PCIe main board.				
FPGAs and Memory	One programmable FPGA (Xilinx Virtex 4 SX XC4VSX55), plus FPGA and memory resources on main board.				
Graychips	Four programmable or optional none (TI GC4016)				
Sample Clock	User-configurable & phase-locked to 10 MHz reference	Tuning range = 10 to 250 MHz			
ADCs (one per port)	Resolution / maximum sample rate	12 bits / 250 MHz			
Data Rates	Dependent on such factors as data format, main board, and system variables.				
Data Format (I/O)	Two configurable data inputs are included, supporting the data formats shown below. (For external reference input, see next heading.) One time code input is also included (1 pps, IRIG-B, or other input, with user-configurable output).				
	PORT 0	**IDM: IF direct module**	**IMM: IF mixer module**		
	Frequency range / center	10 MHz minimum / None	140 or 160 MHz / 55 MHz		
	-3 dB bandwidth	Determined externally	Determined externally		
	Filter options	90 MHz lowpass filter	n/a		
	Input impedance	75 or optional 50 ohms	75 or optional 50 ohms		
	Return loss	16 dB	16 dB		
	Signal level (usable / max)	-45 to -17 / 0 dBm	-65 to -20 / 0 dBm		
	Typical SNR / SFDR	70 / 45 dB	70 / 45 dB		
	PORT 1	**IDM: IF direct module**	**IMM: IF mixer module**	**LBM: L-band module**	
	Frequency range / center	10 MHz minimum / None	140 or 160 MHz / 55 MHz	900 to 2250 MHz / 187.5 MHz	
	-3 dB bandwidth	Determined externally	Determined externally	104 MHz	
	Filter options	90 MHz lowpass filter	n/a	n/a	
	Input impedance	75 or optional 50 ohms	75 or optional 50 ohms	75 ohms	
	Return loss	16 dB	16 dB	16 dB	
	Signal level (usable / max)	-45 to -17 / 0 dBm	-65 to -20 / 0 dBm	-35 to -4 / 0 dBm	
	Typical SNR / SFDR	70 / 45 dB	70 / 45 dB	70 / 50 dB	
External Reference	**10 MHz (input):** Impedance 50 ohms; return loss 12 dB; signal level 0 to 7 dBm usable (11 dBm maximum)				
Internal Reference	**10 MHz (TCXO):** Frequency adjustment range +/– 3 ppm; tolerance +/– 0.5 ppm at 25° C; over temperature +/– 2.5 ppm at 0° to 75° C				
Local Oscillators		**IDM**	**IMM**	**LBM (oscillator 1)**	**LBM (oscillator 2)**
	Tuning range	n/a	215 or 195 MHz (fixed)	1700-2950 MHz	562.5 MHz (fixed)
	Tuning step size	n/a	n/a	1 MHz	n/a
Connectors	Time code, 7-pin Lemo; external reference, SMB 50 ohms; IDM and IMM modules, SMB 50 or 75 ohms; LBM module, F-type 75 ohms.				
Cabling	Consult EDT for purchase options:				
	To 7-pin Lemo on board, from time code source	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)			
Physical	Weight	4.9 oz. typical			
	Dimensions	6.6 x 4.2 x 0.75 in. (with a main board)			
Environmental	Temperature (operating / non-operating)	0° to 40° C / -40° to 70° C			
	Humidity (operating / non-operating)	1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C			
System and Software	System requirements and EDT-provided software driver packages are discussed in the specifications for your EDT main board.				

Ordering Options

- Main board: PCI GS or PCIe8 LX / FX / SX
- Ports 0 and 1: IDM / IMM / LBM (on 1 only)
- Connectors: 50 / **75 ohms** (IF)
- Cabling (for time code input): DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.

Contact

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