User's Guide

PCIe8g3 S5 Family

PCIe Gen3 x8 boards with Stratix V FPGA and 10G / 40G ports

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Contents

PCIe8g3 S5 Family

Overview

The PCIe8g3 S5 (“S5”) family is a group of multiport, multirate interfaces. Currently this family includes two versions...

- The S5 10G – so named because it can support up to four 10G transceivers.
- The S5 40G – so named because it can support one 40G transceiver, plus two 10G transceivers.

Each version includes...

- One Altera Stratix V GX FPGA, with multiple options available;
- One eight-lane PCIe Gen 3 DMA interface;
- Two independent 4 GB banks of DDR3 DRAM, for a total of 8 GB;
- Four programmable oscillators (one per port);
- Support for a jitter-attenuated recovery clock; and
- A variety of transceiver options.

Table 1 shows the transceiver options (by port) for each version.

Table 1. S5 10G and 40G – options by port

S5	Port	DMA channel	Transceiver	Wavelength(s)	Signal(s)*
10G	0	0	SFP	1550, 1310, 850 nm	1GbE; OC3/12/48 (STM1/4/16); OTU1
			SFP+	1550, 1310 nm	10GbE; OC 192 (STM64); OTU2/2e/2f
			SFP+	850 nm	10GbE only
	1	1	[same as port 0]		
	2	2	[same as port 0]		
	3	3	[same as port 0]		
40G	0	0	SFP	1550, 1310, 850 nm	1GbE; OC3/12/48 (STM1/4/16); OTU1
			SFP+	1550, 1310 nm	10GbE; OC 192 (STM64); OTU2/2e/2f
			SFP+	850 nm	10GbE only
	1	1	[same as port 0]		
	4	0 (when `sel_port` = 4)	QSFP+	850 nm	40GbE

* SONET (OC3/12/48) and SDH (STM1/4/16) signal names are used interchangeably.
For signal standards, see Related Resources on page 8.
For port locations and other board features, see Hardware on page 15.

Related Resources

To find product-specific information that is related to a particular EDT product, go to www.edt.com and open the relevant product page. There you'll see links to that product's datasheet (specifications), user's guide, and other resources.

The resources may be helpful or necessary for your applications.

EDT Resources

• Application programming interface (API)	www.edt.com/api/
• Installation packages (Windows, Linux, Mac)	www.edt.com/software
• PCIe8g3 S5-10G datasheet (specifications)	www.edt.com/pcie8g3s5-10g.html
• PCIe8g3 S5-40G datasheet (specifications)	www.edt.com/pcie8g3s5-40g.html
• Time Distribution datasheet (specifications) / user's guide	www.edt.com/timedist.html
• Static Discharge Kit instructions	www.edt.com/static

Third-Party Resources

Standards / Specifications

• PCI Express (PCIe)	www.pcisig.com
• IRIG-B	irigb.com
• International Telecommunications Union (ITU) / Optical Transport Network (OTN) / G.709/Y.133103/2003	www.itu.int
• Ethernet framing (IEEE 802-3)	www.ieee802.org/3/

Parts

• FPGA: Altera Stratix V GX	www.altera.com

Care and Cautions

Although EDT products are built to specifications which allow them to withstand a variety of extreme conditions, they are still high-performance components which require proper care for best results. To protect them and your equipment, follow all recommended instructions for care and cautions, including those in the EDT-provided static discharge kit.

For links to datasheet specifications and EDT static discharge kit instructions, see Related Resources.

Installation and the EDT Installation Package

To physically install your S5 board, follow the steps below while referring to Hardware on page 15.

1. Since each transceiver can be unique, notate the position of each transceiver on your S5 board so you can return each one to its proper place later.
2. Remove the transceivers to enable the board to be inserted into the host system.
3. Insert the board into the host system.
4. Working through the back panel on the host system, return each transceiver to its original position on the S5 board.

NOTE We recommend powering off the board before replacing any transceiver, despite manufacturers' claims that transceivers are hot-swappable.

Now you're ready to review the resources included in the EDT installation package. In addition to the files listed below, custom FPGA configuration files can be requested.

The PCD Device Driver

Your EDT installation package contains the PCD device driver – the software that runs on the host computer and allows the host operating system to communicate with the S5. The driver is loaded into the kernel at installation and thereafter runs as a kernel module. The driver name and subdirectory is specific to each supported operating system, and the installation script automatically installs the appropriate device driver in the appropriate way for your operating system.

Firmware: FPGA Configuration (.bit) Files

Your EDT installation package includes firmware in the form of FPGA configuration (`.bit`) files. The correct `.bit` file for your specific S5 board and FPGA is located and loaded as below.

To find the correct FPGA configuration (.bit) file for...	Look in the flash subdirectory bearing your FPGA part #	For the .bit file named	Which is loaded...
The FPGA on your S5 board	`flash/`*`FPGApart#`*	`pe8s5_4p.bit`	Automatically, from flash memory

If you need to reload the firmware due to corruption or an update, see Configuring the S5 on page 11.

Applications and Utilities

In addition to the above resources, the EDT installation package includes application and utility files that you can use to initialize and configure the board, access the registers, and perform basic testing. In many cases, C or C++ source is provided so that you can use the files as starting points to write your own applications. The most commonly useful files are described below.

NOTE For a link to the latest installation packages, see Related Resources on page 8. For new installations, use the latest package. For existing applications, to avoid version problems, upgrade only if you have a specific reason to do so.

These S5-specific files are included in the `libs5` or `libocx` directory of your EDT installation package...

`fourp`	Utility to set up and initialize the S5.
`fourp.cpp`	Source file for the `fourp` utility.
`EdtS5Xcvr.cpp`	C++ object describing EDT Stratix 5 FPGA's transceiver.
`EdtS5Xcvr.h`	Include file for the above C++ object.
`EdtS5Mem.cpp`	C++ object describing EDT Stratix 5 DDR3 memory and data flow.
`EdtS5Mem.h`	Include file for the above C++ object.
`EdtS5.cpp`	C++ object describing any EDT board based on Stratix 5 FPGA.
`EdtS5.h`	Include file for the above C++ object.
`Edt4P.cpp`	C++ object describing EDT S5 board.
`Edt4P.h`	Include file for the above C++ object.
`edt_fourp.h`	Include file.

In the future, the S5 is scheduled to be supported by such additional applications as...

`OCXSnap`	Example application that captures data from the S5 board and transfers it to disk for testing or verification.
`OCXSnap.cpp`	C source for `OCXSnap.`
`OCXPlay`	Example application that outputs the data captured by `OCXSnap` from the disk for testing or verification.
`OCXPlay.cpp`	C source for `OCXPlay.`
`ReadXFPSFP`	Example application that queries the state of the transceiver modules. For details, see Initializing Ports on page 13.
`ReadXFPSFP.cpp`	C source for `ReadXFPSFP.`
`EdtSFP.cpp`	C library routines used by `ReadXFPSFP` or available for you to use in your own application.
`EdtSFPPlus.cpp`	C library routines used by `ReadXFPSFP` or available for you to use in your own application.

Sample Applications

`rd16`	For DMA channels – performs simple multichannel ring buffer input.
`wr16`	For DMA channels – performs simple multichannel ring buffer output.
`simple_read`	Performs DMA input without using ring buffers. Data is therefore subject to interruptions, depending on system performance.
`simple_write`	Performs DMA output without using ring buffers. Data is therefore subject to interruptions, depending on system performance.

`simple_getdata`	Serves as an example of a variety of DMA-related operations, including reading the data from the connector interface and writing it to a file, as well as measuring input rate.
`simple_putdata`	Serves as an example of a variety of DMA-related operations, including reading data from a file and writing it out to the connector interface.
`test_timeout`	In typical operation, timeouts cancel DMA transfers. This application exemplifies giving notification of timeouts, without canceling DMA.

Utilities

`gstemp`	Utility for monitoring the temperature of the S5.
`pdb`	Enables interactive reading and writing of the UI FPGA registers.
`set_si570`	Programs the S5 reference clock(s) to specific frequencies used by the S5 FPGA for input and output.
`timing_test`	Tests the timecode input.

Building or Rebuilding an Application

In your EDT installation package, executable and PCD source files are in the top-level directory. Therefore, if you need to build or rebuild an application, run `make` in that directory.

Windows users must install a C compiler; we recommend the Microsoft Visual C compiler for Windows. Linux users can use the `gcc` compiler typically included with the Linux installation. If you use Windows and you wish to use `gcc`, contact tech@edt.com.

After you build or rebuild an application, use the `--help` command line option for a list of usage options and descriptions.

Configuring the S5

The S5 has one FPGA, called the PCIe FPGA. This section explains how to...

1. Find the unit number (by default, 0) assigned to your S5 board by your system.
2. Configure the FPGA with the appropriate FPGA configuration file.
3. Configure the physical ports and the DMA channels.

To implement these steps and conduct loopback testing (see Basic Testing [main section - was between Framing and Hardware - no looptest now, but will be later] on page 49), use this section.

To begin data acquisition, further initialization is required (see Initialization and Setup on page 13).

Unit Number

To see which EDT unit(s) are in your host system and to find their unit numbers, run...

```
pciload
```

...with no arguments, and the screen will display information about each one.

FPGA

At power-on, the firmware (FPGA configuration or `.bit` file) is installed automatically via nonvolatile flash memory. Typically you do not need to reconfigure or update the firmware unless...

- you are asked to do so by EDT during a support call or email exchange;
- you install a new driver; or
- the firmware becomes corrupted.

To verify the loading of the correct FPGA configuration file for your S5 board...

1. Navigate to the directory in which you installed the driver. The default locations are...
   - For Windows, `\EDT\pcd`
   - For Linux or Mac, `/opt/EDTpcd`
2. At the prompt, enter...

   ```
   pciload verify
   ```

   ...to compare the FPGA configuration file in the installation package with the one already loaded in flash memory. If multiple boards are installed, enter the unit number after the `-u` option...

   ```
   pciload -u unit number verify
   ```

   If the dates and revision numbers match, there is no need to upgrade. If they differ, you can proceed through the steps below to upgrade the flash memory.
3. At the prompt, enter...

   ```
   pciload update
   ```
4. Shut down the operating system; turn the host computer off, and then on again. The board reloads firmware from flash memory only during powerup. Thus, after running `pciload,` the new FPGA configuration file is not in the FPGA until the system has been power-cycled; simply rebooting is not adequate.

Initialization and Setup

PCIe8g3 S5 boards can be initialized and set up with the `fourp` utility. The recommended sequence is:

1. Initialize the DDR3 memory and set up the data path.
2. Initialize the ports as needed.

NOTE Some setup (such as of the memory and data path) affects all channels, so implement setup with caution.

Initializing Memory and Data Path

To prepare for DMA, the data path must be initialized. Doing so includes setting the data path direction, determining whether data will be directed to DMA, and verifying that the DDR3 memory PHY has been initialized.

In the default FPGA configuration file provided with your S5 board, the two DDR3 memory banks are divided into two logical memory banks. In register 0x000010 Data Path and Memory Control, when port 0, 1, 2, or 3 is set, each port thus set is assigned a logical memory bank; when port 4 is set, then the four logical memory banks are combined into a single logical bank. In the same register, the latter result can be achieved with the `fourp` utility by entering...

```
fourp -rm -p 0 -D -rx
```

...where the flags have the following effects...

- The `-rm` flag resets the DDR3 PHY.
- The `-p 0` flag sets the memory for ports 0, 1, 2, and 3.
- The `-D` flag sets the data path for DMA.
- The `-rx` flag sets the data path for receiving data.

NOTE The `-D` flag always should be used with either the `-rx` or the `-tx` flag (`-rx` and `-tx` are mutually exclusive) and will affect all ports.

Initializing Ports

Each port can be set up and used independently by using the `fourp` utility and adding the flags...

```
-p x  // to determine which port is configured;
-R x  // to determine which rate is set.
```

For example, you could enter these three commands, in any sequence...

```
fourp -p 0 -R stm64
fourp -p 1 -R otu2f
fourp -p 2 -R stm1
```

...in order to set port 0 to STM64, port 1 to OTU2f, and port 2 to STM1.

NOTE When you specify a rate, the `fourp` utility does not verify whether a port's transceiver can support that rate. Therefore, you must be aware of which transceiver is in each port (the board can read this information for you) and what each transceiver's capabilities are.

Using the `fourp` utility in this way will set the respective port's reference clock and reconfigure the FPGA's SERDES appropriately; however, it will not set up the relevant port's framing register (0x800000, 810000, 820000, 830000 Receive Framer Status and Control) or demux bitmap register (0x80003C, 81003C, 82003C, 83003C Demux Bitmask), nor will it enable the relevant channel for DMA in registers 0x00 Command and 0x10–11 DMA Channel Enable.

Querying the Transceivers

To query the transceiver on a specified port, you can use `fourp -p x` with these flags...

```
-w // to query the received optical power
-C // to query the temperature
```

For example, you could enter such commands as...

```
fourp -p 0 -C // to query port 0 for received optical power
fourp -p 1 -w // to query port 1 for temperature
```

...without disrupting the other ports or the DMA.

For details, see the manufacturer's website for the transceivers you are using (see Related Resources on page 8).

Time Code

The S5 uses the same timecode interface as the EDT Time Distribution board. For details, see these registers...

- Register 0x6D SPI Data
- Register 0x6E SPI Status and Control
- Register 0x6F SPI Strobe

...and consult the Time Distribution user's guide (Related Resources on page 8).

Framing

The S5 default firmware (FPGA configuration file) supports framing capabilities as described below.

For 10GbE and 40GbE, currently only clear-bit data is supported.

For OTN and OC / STM, framing headers are included in the data transferred during DMA. If framing is enabled, the board searches and locks onto incoming SONET / SDH frames after detecting the presence of A1 and A2 header patterns at 125 ms intervals. The algorithm sequence is:

1. *Search.* The board searches for A1 and A2 header patterns until it sees a match; then it goes to *Check*.
2. *Check.* The board checks for three consecutive SONET / SDH frames at 125-microsecond intervals with the A1 and A2 header patterns in the proper position, before declaring *Lock*.
3. *Lock.* Once locked, incoming SONET / SDH frames are collected and forwarded to the host. The board continues to check for the A1 and A2 header patterns, and remains in this state until the A1 and A2 header patterns are lost. When the patterns are lost, it enters the *Flywheel* state.
4. *Flywheel.* If the A1 and A2 header patterns are not seen for three consecutive frames, the board returns to *Search*; if it finds them, it returns to *Lock*. SONET / SDH frames are collected and forwarded to the host in this state as well.

Hardware

The S5 works as a standalone board. Block diagrams and ports for both versions (10G and 40G) are shown below.

Block Diagrams

Figure 1 and Figure 2 show the respective architecture of the 10G version and the 40G version.

Figure 1. S5 10G

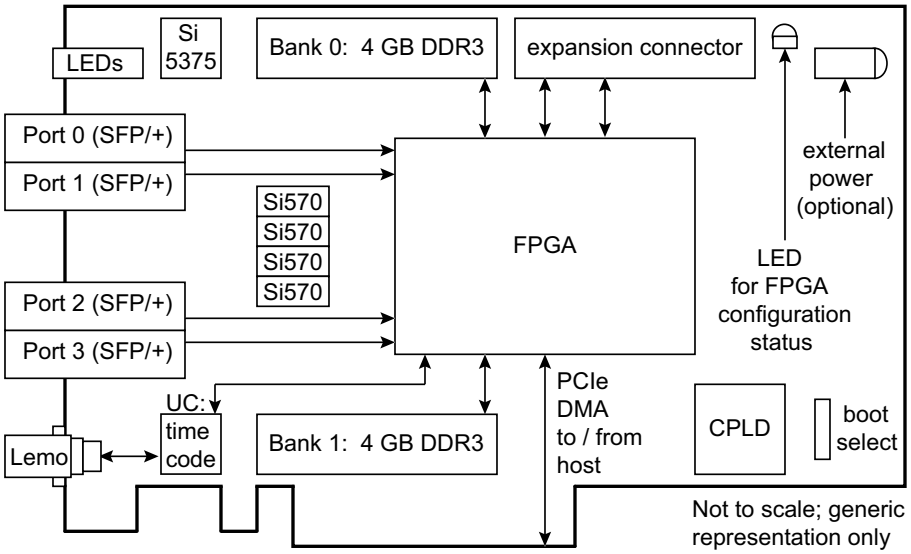
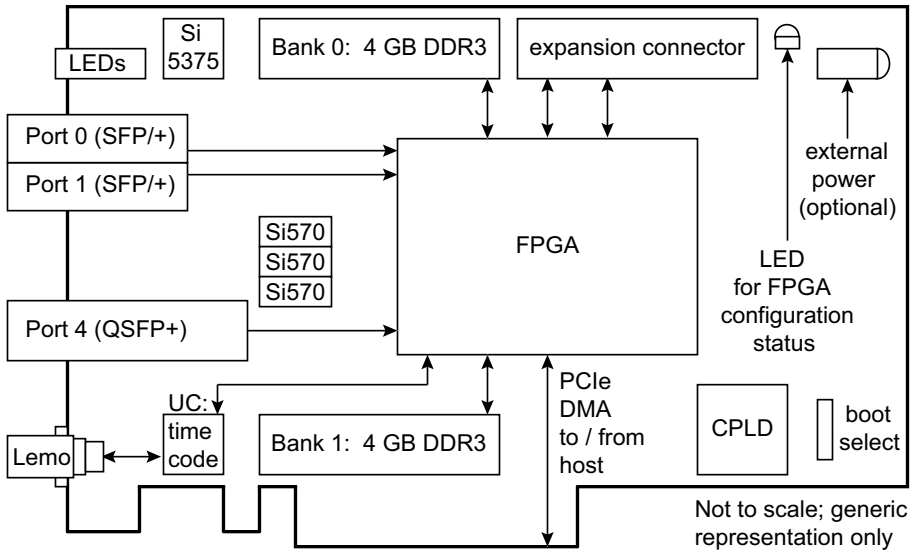


Figure 2. S5 40G



Ports and LED Status Indicators

Figure 3 and Figure 4 show closeup images of the connectors and the LED status indicators.

Figure 3. S5 10G ports and LED status indicators

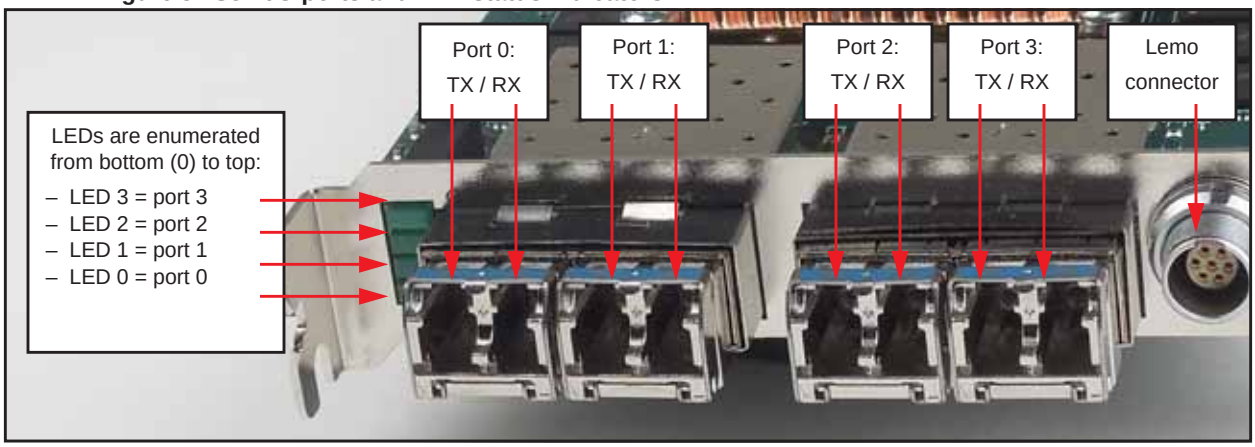
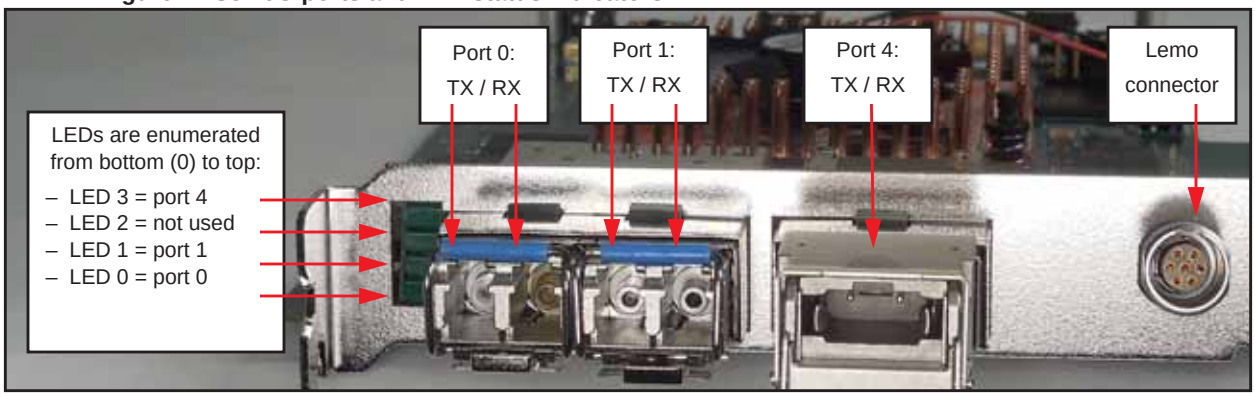


Figure 4. S5 40G ports and LED status indicators



Each LED indicates the status of its respective port – namely, whether the port is ready to receive, is receiving, and is framing a signal. If a port is working properly in all three areas, its LED is steady green. If not, its LED will be blinking.

Table 2 summarizes the LED behaviors.

Table 2. LED behaviors

LED behavior	FPGA receive clock locked / ready to receive?	Signal being received?	Signal being framed?
Dim blinking	No	No	No
Bright blinking	Yes	Yes	No
Bright steady	Yes	Yes	Yes

APPENDIX A: Registers for PCIe8g3 S5

For the PCIe8g3 S5 10G/40G, the registers are divided into two main categories and register spaces:

- the user interface (UI) register space, for functions that are not port-specific; and
- the port register space, for functions that are port-specific.

Each space contains both indirect and BAR1 memory-mapped registers, and the port register space is further divided so each port has its own indirect and BAR1 registers. The addresses are shown in Table 3.

Table 3. Addresses – UI and port registers (indirect and BAR1 memory-mapped)

	Indirect	BAR1 memory-mapped
UI registers (non–port-specific)		
Any port	0x00–0x7F	0x000000–0x7FFFFF
Port registers (port-specific)		
Port 0	0x80–0x87	0x800000–0x807FFF
Port 1	0x88–0x8F	0x810000–0x817FFF
Port 2	0x90–0x97	0x820000–0x827FFF
Port 3	0x98–0x9F	0x830000–0x837FFF
Port 4	0xA0–0xA7	0x840000–0x847FFF

The port registers are defined for port 0, and since each of the other ports has identical registers within its respective memory space, a C macro is included in `edt_stratix5.h` to help you locate a specific register related to a specific port. The macro, which works for both indirect and BAR1 memory-mapped addresses, is defined as...

STRATIX5_REGXL8(*register_address, port_number*)

...with the italicized variables being replaced by the appropriate register address and port number, as shown in the access information provided with each register below.

Registers, UI

0x00–0x7F Indirect

0x00 Command

		Access / Notes:	8-bit read-write / PCD_CMD
Bit	**Access**	**Name**	**Description**
7–4	RW	PCD_STAT_INT_EN	Enables interrupts as defined in registers 0x03 Interrupt Status and 0x04 Interrupt Enable.
3	RW	CMD_EN	Set this bit to enable the required DMA channels in 0x10–11 DMA Channel Enable for DMA. When clear, resets all DMA channels, flushes all FIFOs, and clears all under- and overflow bits.
2–0	–	–	Reserved.

0x03 Interrupt Status

		Access / Notes:	8-bit read-only / PCD_STAT This register is connected to 1Hz test interrupt as an example of interrupts generated by the UI FPGA on the main board.
Bit	**Access**	**Name**	**Description**
7–4	R only	PCD_STAT_INT	Interrupt bits for the status bits. If the corresponding bit is asserted in 0x00 Command, then the corresponding bit of these four can be asserted to cause a PCI bus interrupt. The PCI bus interrupt then is caused when the corresponding PCD_STAT signal [bits 3–0] is asserted. To reset the interrupt, disable and re-enable the appropriate PCD_STAT_INT_EN bit [7–4] in 0x00 Command.
3–0	R only	PCD_STAT	The state of user-definable STAT input signals as last sampled.

0x04 Interrupt Enable

		Access / Notes:	8-bit read-write / PCD_STAT_POLARITY This register is connected to 1Hz test interrupt as an example of interrupts generated by the UI FPGA on the main board.
Bit	**Access**	**Name**	**Description**
7–5	–	–	Reserved.
4	RW	PCD_STAT_INT_ENA	Provides global enable or disable for all interrupt bits [7–4] in 0x03 Interrupt Status above, allowing the driver to disable and re-enable them in one operation without altering their states. A value of 1 enables the interrupts; a value of 0 disables them.
3–0	–	[no name]	Reserved.

0x0D Exended Configuration

Access / Notes: 8-bit read-write / PCD_EXT_CONFIG

Registers 0x0D, 0x0F, and 0x16 all can affect how data is ordered.

Bit	Access	Name	Description
7–1	–	[no name]	Reserved.
0	RW	WSWAP	Word swap bit; swaps two 32-bit words in one 64-bit data word, so that word 0 is transferred before word 1. Does not change the position of the bits within each word.

0x0F Configuration

Access / Notes: 8-bit read-write / PCD_CONFIG

Registers 0x0D, 0x0F, and 0x16 all can affect how data is ordered.

Bit	Access	Name	Description
7–4	–	–	Reserved.
3	RW	SSWAP	Short swap bit; swaps the two 16-bit short words in one 32-bit data word, so that short 0 is transferred before short 1. Does not change the order of the bits within each short.
2–1	–	–	Reserved.
0	RW	BSWAP	Byte swap bit; swaps bytes 0 and 1, and also bytes 2 and 3, in a 32-bit data word, so that the bytes are positioned 1, 0, 3, 2. Does not change the position of the bits within each byte.

Below is the structure of a 64-bit data word, with no swapping in effect.

Bits:	63–56	55–48	47–40	39–32	31–24	23–16	15–8	7–0
Bytes:	7	6	5	4	3	2	1	0
Shorts:	3		2		1		0	
Words:	1				0			

Below are the data ordering sequences achieved by setting or unsetting, in various combinations, the bits WSWAP, SSWAP, and BSWAP.

WSWAP	SSWAP	BSWAP	Resultant Byte Order
0	0	0	7, 6, 5, 4, 3, 2, 1, 0
0	0	1	6, 7, 4, 5, 2, 3, 0, 1
0	1	1	4, 5, 6, 7, 0, 1 2, 3
1	1	1	0, 1, 2, 3, 4, 5, 6, 7
0	1	0	5, 4, 7, 6, 1, 0, 3, 2
1	0	0	3, 2 1, 0, 7, 6, 5, 4

0x10–11 DMA Channel Enable

		Access / Notes:	16-bit read-write / SSD16_CHEN
Bit	**Access**	**Name**	**Description**
15–0	RW	CH_ENABLE[15–0]	Set or clear the appropriate bit to enable or reset the corresponding DMA channel: - Set bit 12 to transmit data to port 4; clear to reset. - Set bit 11 to transmit data to port 3; clear to reset. - Set bit 10 to transmit data to port 2; clear to reset. - Set bit 9 to transmit data to port 1; clear to reset. - Set bit 8 to transmit data to port 0; clear to reset. - Set bit 4 to receive data from port 4; clear to reset. - Set bit 3 to receive data from port 3; clear to reset. - Set bit 2 to receive data from port 2; clear to reset. - Set bit 1 to receive data from port 1; clear to reset. - Set bit 0 to receive data from port 0; clear to reset.

0x16–17 Least Significant Bit First

		Access / Notes:	16-bit read-write / SSD16_LSB Registers 0x0D, 0x0F, and 0x16 all can affect how data is ordered.
Bit	**Access**	**Name**	**Description**
15–0	RW	LSB_FIRST[5–0]	When set for a DMA channel, the least significant bit of the 32-bit data word is first, and the most significant bit is last; when clear, the most significant bit of a 32-bit word is first.

0x18–19 Underflow

		Access / Notes:	16-bit read-only / SSD16_UNDER
Bit	**Access**	**Name**	**Description**
15–0	R only	UNDERFLOW[12 –0]	A value of 1 in a bit indicates that the corresponding DMA channel's internal FIFO has underflowed since the channel was last enabled. Underflow causes the corresponding DMA channel to transmit the last valid byte repeatedly until it receives new DMA data. To reset, clear and reenable the appropriate channel (see 0x00 Command and 0x10–11 DMA Channel Enable).

0x1A–1B Overflow

		Access / Notes:	16-bit read-only / SSD16_OVER
Bit	**Access**	**Name**	**Description**
15–0	R only	OVERFLOW[12–0]	A value of 1 in a bit indicates that the corresponding DMA channel's internal FIFO has overflowed since the channel was last enabled. Data received while the FIFO is in overflow is discarded. To reset, clear and reenable the appropriate channel (see 0x00 Command and 0x10–11 DMA Channel Enable).

0x60–62 Extended Indirect Register Address

		Access / Notes:	24-bit read-write / [no name] 0x60 = bits 7–0; 0x61 = bits 15–8; 0x62 = bits 23–16.
Bit	**Access**	**Name**	**Description**
23–0	RW	[no name]	This is the register address space for the extended indirect registers.

0x63 Extended Indirect Register Data

		Access / Notes:	8-bit read-write / [no name]
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	This is the register data for the extended indirect registers. – Writing this register writes data to the register addressed by 0x60–62. – Reading this register reads the data addressed by 0x60–62.

0x64 Serial Master Interface Status

		Access / Notes:	8-bit read-write / STRATIX5_I2C_DEVICE
Bit	**Access**	**Name**	**Description**
7	R only	SER_DEV_BSY	When set, the serial master is busy.
6	R only	SER_DEV_ACK_FAIL	When set, the serial slave failed to respond to the last command.
5–0	RW	SER_DEV_ADDR	Descriptions for devices 0–20 are provided below. 0 = Port 0 reference clock (Si570). 1 = Port 1 reference clock (Si570). 2 = Ports 2 and 4 reference clock (Si570). 3 = Port 3 reference clock (Si570). 4 = Port 0 external PLL (Si5375). 5 = Port 1 external PLL (Si5375). 6 = Port 2 external PLL (Si5375). 7 = Port 3 external PLL (Si5375). 8 = Port 0 SFP/+ EEPROM. 9 = Port 1 SFP/+ EEPROM. 10 = Port 2 SFP/+ EEPROM and Port 4 QSFP EEPROM. 11 = Port 3 SFP/+ EEPROM. 12 = Port 0 SFP/+ diagnostics. 13 = Port 1 SFP/+ diagnostics. 14 = Port 2 SFP/+ diagnostics. 15 = Port 3 SFP/+ diagnostics. 16 = Port 0 SFP active copper PHY. 17 = Port 1 SFP active copper PHY. 18 = Port 2 SFP active copper PHY. 19 = Port 3 SFP active copper PHY. 20 = U2M reference clock (Si5375).

0x65 Serial Master Interface Read [7–0]

		Access / Notes:	8-bit read-write / STRATIX5_I2C_READ_ADDR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	This register [bits 7–0] works with 0x68 Serial Master Interface Read [15–8]. Write the register address on the serial slave that you wish to read. Read the data returned from the register address.

0x66 Serial Master Interface Register Address [7–0]

		Access / Notes:	8-bit read-write / STRATIX5_I2C_WRITE_ADDR
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	This register [bits 7–0] works with 0x69 Serial Master Interface Register Address [15–8]. Write the register address on the serial slave that you wish to read. Read the register address.

0x67 Serial Master Interface Write [7–0]

		Access / Notes:	8-bit read-write / STRATIX5_I2C_WRITE_DATA
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	This register works [bits 7–0] with 0x6A Serial Master Interface Write [15–8]. Write data to the serial slave.

0x68 Serial Master Interface Read [15–8]

		Access / Notes:	8-bit read-write / STRATIX5_I2C_READ_DATA_UPPER
Bit	**Access**	**Name**	**Description**
15–8	R only	[no name]	This register [bits 15–8] works with 0x65 Serial Master Interface Read [7–0]. Write the register address on the serial slave that you wish to read. Read the data returned from the register address.

0x69 Serial Master Interface Register Address [15–8]

		Access / Notes:	8-bit read-write / STRATIX5_I2C_WRITE_ADDR_UPPER
Bit	**Access**	**Name**	**Description**
15–8	RW	[no name]	This register [bits 15–8] works with 0x66 Serial Master Interface Register Address [7–0]. Write the register address on the serial slave that you wish to read. Read the register address.

0x6A Serial Master Interface Write [15–8]

		Access / Notes:	8-bit read-write / STRATIX5_I2C_WRITE_DATA_UPPER
Bit	**Access**	**Name**	**Description**
15–8	RW	[no name]	This register [bits 15–8] works with 0x67 Serial Master Interface Write [7–0]. Write data to the serial slave.

0x6B Reference Clock Control

		Access / Notes:	8-bit read-write / STRATIX5_EXT_PLL
Bit	**Access**	**Name**	**Description**
7	RW	[no name]	Assert to reset the external PLL for all four interfaces.
6–4	–	–	Reserved.
3–0	RW	[no name]	Set to select the local reference crystal as the source for each respective interface on the external PLL; otherwise, use the recovered clock as the source. Bit 3 = Port 3 Bit 2 = Port 2 Bit 1 = Port 1 Bit 0 = Port 0

0x6C Sync Trigger Control and Status

		Access / Notes:	8-bit read-write / STRATIX5_SYNC_REG
Bit	**Access**	**Name**	**Description**
7–5	–	–	Reserved.
4	R only	STRATIX5_SYNC_IN	Status of external synchronization trigger.
3–1	–	–	Reserved.
0	RW	STRATIX5_SYNC_OUT	Set to send the synchronization trigger.

0x6D SPI Data

		Access / Notes:	8-bit read-write / SPI_DATA
Bit	**Access**	**Name**	**Description**
7–0	RW	[no name]	If read, bits read from the input FIFO. If written, bits write to the output FIFO.

0x6E SPI Status and Control

		Access / Notes:	8-bit read-write / SPI_STAT_CTRL
Bit	**Access**	**Name**	**Description**
7	R only	CHIP_ENABLE	Detects which main board is connected to the S5 master header. A value of 1 indicates the master header; otherwise reads 0.
6	R only	IRIGB_PULSE_IN	If set, indicates that the 1 pps signal has been detected from the incoming IRIG signal, and has been processed by and passed through the microcontroller.
5	R only	MODEM_PULSE_IN	If set, indicates that the 1 pps signal has been detected from the satellite modem and passed directly through, without any processing by the microcontroller.
4	–	[no name]	Reserved; reads as 0.
3	R only	FIFO_OUT_EMPTY	If set, indicates the output FIFO is empty.
2	R only	FIFO_OUT_FULL	If set, indicates the output FIFO is full.
1	R only	FIFO_IN_EMPTY	If set, indicates the input FIFO is empty.
0	RW	If written: RESET If read: FIFO_IN_OV	On write: toggle this bit to reset the SPI data path. On read: when set, indicates the input FIFO has overflowed. Data may be lost.

0x6F SPI Strobe

		Access / Notes:	8-bit write-only / SPI_STROBE
Bit	**Access**	**Name**	**Description**
7–0	W only	[no name]	Write (any value) to this register to advance the input FIFO.

0x7C–7D FPGA Configuration File Design ID

		Access / Notes:	16-bit read-only / PCD_DESIGN_ID
Bit	**Access**	**Name**	**Description**
15–0	R only	[no name]	A 16-bit number assigned by the organization that produced the FPGA configuration file loaded in the main board UI FPGA. The design ID for `pe8s5_40g.bit` is 0x1C00. The design ID for `pe8s5_4p.bit` is 0x1C04.

0x7E FPGA Configuration File Version String

		Access / Notes:	8-bit read-write / MAIN_BITFILE_VERSION To read the FPGA configuration file version string from ROM, write the ROM address to the register and read the ASCII data from the same register. The version string is a maximum of 64 bytes long, so only the first six bits of the address are significant.
Bit	**Access**	**Name**	**Description**
7–0	RW	ID_ADD_DATA	Write an address to read ROM contents. Result is... *`mainBoard_mezzBoard_bitfileName version.revision mm/dd/yyyy (number of DMA channels used, number of DMA channels required by PCI FPGA)`* *`mm/dd/yyyy`* is the date the FPGA configuration file was created. Replace italicized terms with actual values — for example, `sv16_pe8s5_4p 0.0 04/24/2013 (10,10).`

0x7F Board ID [Reserved]

Registers, UI

0x000000–0x7FFFF BAR1 Memory-Mapped

0x000010 Data Path and Memory Control

		Access / Notes:	32-bit read-write / STRATIX5_MEMPATH_CTRL
Bit	**Access**	**Name**	**Description**
31–25	–	–	Reserved.
24	RW	STRATIX5_MEM_LOOP_MODE	Assert to enable loop mode to allow for looping in DDR3 memory. Use in conjunction with register 0x000024 Memory Loop Size.
23-20	RW	[no name]	Select port (data source for memory).
19–17	–	–	Reserved.
16	RW	STRATIX5_SEL_DMA	Assert to direct data to DMA.
15	RW	STRATIX5_MEM_SYNC_DIMM	Assert to synchronize the DDR3 memory banks, effectively creating a single, wider bank of memory.
14	RW	STRATIX5_MEM_WR_FIRST	Assert to set write priority for memory.
13	RW	STRATIX5_MEM_M1_ACTIVE	Memory port 1 active.
12	RW	STRATIX5_M0_BYPASS	Memory port 0 bypass mode.
11	R only	[no name]	Bank D PHY initialization completed successfully.
10	R only	[no name]	Bank C PHY initialization completed successfully.
9	R only	[no name]	Bank B PHY initialization completed successfully.
8	R only	[no name]	Bank A PHY initialization completed successfully.
7	RW	[no name]	Bank D logical reset.
6	RW	[no name]	Bank C logical reset.
5	RW	[no name]	Bank B logical reset.
4	RW	[no name]	Bank A logical reset.
3	RW	[no name]	Bank D PHY reset.
2	RW	[no name]	Bank C PHY reset.
1	RW	[no name]	Bank B PHY reset.
0	RW	[no name]	Bank A PHY reset.

0x000014 Memory Status

		Access / Notes:	32-bit read-only / STRATIX5_DFIFO_STATUS
Bit	**Access**	**Name**	**Description**
31–28	R only	[no name]	Bank D debug information.
27–24	R only	[no name]	Bank C debug information.
23–20	R only	[no name]	Bank B debug information.
19–16	R only	[no name]	Bank A debug information.
15	R only	[no name]	Bank D 100% full.

14	R only	[no name]	Bank D 75% full.
13	R only	[no name]	Bank D 50% full.
12	R only	[no name]	Bank D 25% full.
11	R only	[no name]	Bank C 100% full.
10	R only	[no name]	Bank C 75% full.
9	R only	[no name]	Bank C 50% full.
8	R only	[no name]	Bank C 25% full.
7	R only	[no name]	Bank B 100% full.
6	R only	[no name]	Bank B 75% full.
5	R only	[no name]	Bank B 50% full.
4	R only	[no name]	Bank B 25% full.
3	R only	[no name]	Bank A 100% full.
2	R only	[no name]	Bank A 75% full.
1	R only	[no name]	Bank A 50% full.
0	R only	[no name]	Bank A 25% full.

0x000018 W PRBS [Reserved]

0x00001C W PRBS 2 [Reserved]

0x000024 Memory Loop Size

		Access / Notes:	32-bit read-write / STRATIX5_MEMLOOP_LNGTH
Bit	**Access**	**Name**	**Description**
31–0	RW	[no name]	Memory loop size.

0x000028 Memory Information

		Access / Notes:	32-bit read-only / STRATIX5_MEMINFO
Bit	**Access**	**Name**	**Description**
31–28	–	–	Reserved.
27–20	R only	[no name]	Avalon address width, in bits.
19–10	R only	[no name]	Data word width in bytes per bank.
9–0	R only	[no name]	Burst size in number of transfers (four data words per transfer).

Registers, Port: Ports 0–3 (SFPs)

0x80–0x9F Indirect

0x80, 88, 90, 98 SFP Configuration and Status

Access / Notes: 8-bit read-write

0x80 (Port 0): STRATIX5_REGXL8(STRATIX5_OPT_XCVR, 0)
0x88 (Port 1): STRATIX5_REGXL8(STRATIX5_OPT_XCVR, 1)
0x90 (Port 2): STRATIX5_REGXL8(STRATIX5_OPT_XCVR, 2)
0x98 (Port 3): STRATIX5_REGXL8(STRATIX5_OPT_XCVR, 3)

Bit	Access	Name	Description
7	R only	[no name]	When set, indicates a loss of signal.
6	R only	[no name]	When set, indicates an SFP/+ transmit fault.
5	R only	[no name]	When set, indicates the SFP/+ is connected and detected.
4–3	–	–	Reserved.
2	RW	[no name]	Set for SFP+ rate select (1).
1	RW	[no name]	Set for SFP+ rate select (0).
0	RW	[no name]	Set to disable transmit.

0x82, 8A, 92, 9A Port Status

Access / Notes: 8-bit read-only

0x82 (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_STAT, 0)
0x8A (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_STAT, 1)
0x92 (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_STAT, 2)
0x9A (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_STAT, 3)

Bit	Access	Name	Description
7	–	–	Reserved.
6	R only	[no name]	When set, indicates the transceiver reconfiguration is in progress.
5	–	–	Reserved.
4	R only	[no name]	When set, indicates the transceiver transmit PLL0 is locked.
3	R only	[no name]	When set, indicates the transceiver CDR is locked to data.
2	R only	[no name]	When set, indicates the transceiver CDR is locked to reference clock.
1	R only	[no name]	When set, indicates the transceiver is ready to receive.
0	R only	[no name]	When set, indicates the transceiver is ready to transmit.

0x87, 8F, 97, 9F Port Information

Access / Notes: 8-bit read-only

0x87 (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_INFO, 0)
0x8F (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_INFO, 1)
0x97 (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_INFO, 2)
0x9F (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_INFO, 3)

Bit	Access	Name	Description
7–4	R only	[no name]	Port type (SFP+ = 0; QSFP = 1).
3–0	R only	[no name]	Port number.

Registers, Port: Ports 0–3 (SFPs)

0x800000–0x837FFF BAR1 Memory-Mapped

0x800000, 810000, 820000, 830000 Receive Framer Status and Control

Access / Notes: 32-bit read-write
0x800000 (Port 0): STRATIX5_REGXL8(STRATIX5_RX_FRM, 0)
0x810000 (Port 1): STRATIX5_REGXL8(STRATIX5_RX_FRM, 1)
0x820000 (Port 2): STRATIX5_REGXL8(STRATIX5_RX_FRM, 2)
0x830000 (Port 3): STRATIX5_REGXL8(STRATIX5_RX_FRM, 3)

Bit	Access	Name	Description
31	R only	[no name]	Copy of S5_RXFRM_BYTE_ALGND.
30–28	R only	[no name]	Byte offset.
27	R only	[no name]	Copy of S5_RXFRM_BIT_ALGND.
26–24	R only	[no name]	Bit offset.
23–16	–	–	Reserved.
15	R only	S5_RXFRM_FRM_LCKD	When set, the framer has detected multiple consecutive frames and is locked.
14	R only	S5_RXFRM_FRM_FOUND	When set, the framer has deteced the beginning of an SDH / OTN frame.
13–10	–	–	Reserved.
9	R only	S5_RXFRM_BYTE_ALGND	When set, the framer is byte-aligned to the SDH / OTN frame alignment signal (FAS) pattern.
8	R only	S5_RXFRM_BIT_ALGND	When set, the framer is bit-aligned to the SDH / OTN frame alignment signal (FAS) pattern.
7–5	–	–	Reserved.
4	RW	S5_RXFRM_DIS_DSCRM	Set to disable the descrambler (i.e., acquire framed, scrambled data). Used only in conjunction with bit 1 (S5_RXFRM_EN).
3	RW	S5_RXFRM_CHK_PAYLD	Set to enable hardware checking of PRBS payload data.
2	RW	S5_RXFRM_CAT_PAYLD	Set to capture only payload data (i.e., strip framing).
1	RW	S5_RXFRM_EN	Set to allow data acquisition only when the framer is locked to the incoming signal. Acquired data is descrambled.
0	RW	S5_RXFRM_RST	Reset framer. Set, then clear to force the framer to drop, then relock onto the framing pattern.

0x800004, 810004, 820004, 830004 Receive Filter

Access / Notes: 32-bit read-write
0x800004 (Port 0): STRATIX5_REGXL8(STRATIX5_RX_FILTER, 0)
0x810004 (Port 1): STRATIX5_REGXL8(STRATIX5_RX_FILTER, 1)
0x820004 (Port 2): STRATIX5_REGXL8(STRATIX5_RX_FILTER, 2)
0x830004 (Port 3): STRATIX5_REGXL8(STRATIX5_RX_FILTER, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7	RW	S5_RXFILT_IGNR_ALL_FILT	Set to ignore all filters (overrides all other bits in this register).

6–3	–	–	Reserved.
2	RW	S5_RXFILT_STRIP_FEC	Set to strip FEC (OTU only).
1	RW	S5_RXFILT_ALL_OTU_OVRHD	Set to force capture of OTU overhead (regardless of the demux mask).
0	RW	S5_RXFILT_OVRHD_ONLY	Set to capture only frame overhead data (i.e., strip payload).

0x800008, 810008, 820008, 830008 Transmit Framer Control [Reserved]

0x80000C, 81000C, 82000C, 83000C Line Rate / Protocol Control

Access / Notes: 32-bit read-write

0x80000C (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_RATE, 0)
0x81000C (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_RATE, 1)
0x82000C (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_RATE, 2)
0x83000C (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_RATE, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7–0	RW	[no name]	Set expected line rate / protocol: 0 = STM64 / OC192 1 = STM16 / OC48 2 = STM4 / OC12 3 = STM1 / OC3 4 = 1GbE 5 = 10GbE 6 = OTU2 7 = OTU2e 8 = OTU2F 9 = OTU1

0x800010, 810010, 820010, 830010 Synchronization Control

Access / Notes: 32-bit read-write

0x800010 (Port 0): STRATIX5_REGXL8(STRATIX5_PSYNC_CTRL, 0)
0x810010 (Port 1): STRATIX5_REGXL8(STRATIX5_PSYNC_CTRL, 1)
0x820010 (Port 2): STRATIX5_REGXL8(STRATIX5_PSYNC_CTRL, 2)
0x830010 (Port 3): STRATIX5_REGXL8(STRATIX5_PSYNC_CTRL, 3)

Bit	Access	Name	Description
31–16	–	–	Reserved.
15	RW	STRATIX5_TXTRIG_ARM	Set to arm transmit trigger.
14	–	–	Reserved.
13–12	RW	[no name]	Select when DDR3 FIFO transmit will start: 0 = ignore 1 = when FIFO is 50% full 2 = when FIFO is 75% full 3 = when FIFO is 100% full The transmit logic waits to transmit until the selected threshold is reached.
11–10	–	–	Reserved.

9–8	RW	[no name]	Select transmit trigger source: 0 = external 1 = internal
7	RW	STRATIX5_ RXTRIG_ARM	Set to arm receive trigger.
6–3	–	–	Reserved.
2	RW	[no name]	Set to disable wait for frame receive trigger mode.
1–0	RW	[no name]	Select receive trigger source: 0 = external 1 = internal

0x800014, 810014, 820014, 830014 Frame Statistics Count Control

Access / Notes: 32-bit read-write
0x800014 (Port 0): STRATIX5_REGXL8(STRATIX5_FRM_CNT_CTRL, 0)
0x810014 (Port 1): STRATIX5_REGXL8(STRATIX5_FRM_CNT_CTRL, 1)
0x820014 (Port 2): STRATIX5_REGXL8(STRATIX5_FRM_CNT_CTRL, 2)
0x830014 (Port 3): STRATIX5_REGXL8(STRATIX5_FRM_CNT_CTRL, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7	RW	[no name]	Set to enable the frame statistics counters; clear to reset the counters.
6–1	–	–	Reserved.
0	RW	[no name]	Set to capture frame statistics counter data (B1, B2, M1, LOF); clear to update counters continuously.

0x800018, 810018, 820018, 830018 Transmit National Byte

Access / Notes: 32-bit read-write
0x800018 (Port 0): STRATIX5_REGXL8(STRATIX5_TX_NATIONAL, 0)
0x810018 (Port 1): STRATIX5_REGXL8(STRATIX5_TX_NATIONAL, 1)
0x820018 (Port 2): STRATIX5_REGXL8(STRATIX5_TX_NATIONAL, 2)
0x830018 (Port 3): STRATIX5_REGXL8(STRATIX5_TX_NATIONAL, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7–0	RW	[no name]	The National byte for locally generated SONET / SDH transmit frames.

0x80001C, 81001C, 82001C, 83001C Transmit Test Pattern

Access / Notes: 32-bit read-write
0x80001C (Port 0): STRATIX5_REGXL8(STRATIX5_TX_TEST_PAT, 0)
0x81001C (Port 1): STRATIX5_REGXL8(STRATIX5_TX_TEST_PAT, 1)
0x82001C (Port 2): STRATIX5_REGXL8(STRATIX5_TX_TEST_PAT, 2)
0x83001C (Port 3): STRATIX5_REGXL8(STRATIX5_TX_TEST_PAT, 3)

Bit	Access	Name	Description
31–16	–	–	Reserved.
15–0	RW	[no name]	Set the transmit test pattern.

0x800020, 810020, 820020, 830020 Last B1 Error

Access / Notes: 32-bit read-only
0x800020 (Port 0): STRATIX5_REGXL8(STRATIX5_LAST_B1_ERR, 0)
0x810020 (Port 1): STRATIX5_REGXL8(STRATIX5_LAST_B1_ERR, 1)
0x820020 (Port 2): STRATIX5_REGXL8(STRATIX5_LAST_B1_ERR, 2)
0x830020 (Port 3): STRATIX5_REGXL8(STRATIX5_LAST_B1_ERR, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7–0	R only	[no name]	The value of the error mask for the last B1 error. A B1 error mask is one byte resulting from a logical operation on the previous frame. Errors occurring regularly in the same bit of the byte can indicate a problem in the sender's or receiver's equipment. If errors are occurring on the fiber, the B1bits in error are more likely to be randomly located in the byte.

0x800024, 810024, 820024, 830024 B1 Error Count

Access / Notes: 32-bit read-only
0x800024 (Port 0): STRATIX5_REGXL8(STRATIX5_B1_ERR_CNT, 0)
0x810024 (Port 1): STRATIX5_REGXL8(STRATIX5_B1_ERR_CNT, 1)
0x820024 (Port 2): STRATIX5_REGXL8(STRATIX5_B1_ERR_CNT, 2)
0x830024 (Port 3): STRATIX5_REGXL8(STRATIX5_B1_ERR_CNT, 3)

Bit	Access	Name	Description
31–24	–	–	Reserved.
23–0	R only	[no name]	The number of B1 bits found to be in error since the counter was last reset.

0x800028, 810028, 820028, 830028 B2 Error Count

Access / Notes: 32-bit read-only
0x800028 (Port 0): STRATIX5_REGXL8(STRATIX5_B2_ERR_CNT, 0)
0x810028 (Port 1): STRATIX5_REGXL8(STRATIX5_B2_ERR_CNT, 1)
0x820028 (Port 2): STRATIX5_REGXL8(STRATIX5_B2_ERR_CNT, 2)
0x830028 (Port 3): STRATIX5_REGXL8(STRATIX5_B2_ERR_CNT, 3)

Bit	Access	Name	Description
31–0	R only	[no name]	The number of B2 bits found to be in error since the counter was last reset.

0x80002C, 81002C, 82002C, 83002C M1 Error Count

Access / Notes: 32-bit read-only
0x80002C (Port 0): STRATIX5_REGXL8(STRATIX5_M1_ERR_CNT, 0)
0x81002C (Port 1): STRATIX5_REGXL8(STRATIX5_M1_ERR_CNT, 1)
0x82002C (Port 2): STRATIX5_REGXL8(STRATIX5_M1_ERR_CNT, 2)
0x83002C (Port 3): STRATIX5_REGXL8(STRATIX5_M1_ERR_CNT, 3)

Bit	Access	Name	Description
31–24	–	–	Reserved.
23–0	R only	[no name]	The number of M1 bits found to be in error since the counter was last reset. The M1 byte is sent from the remote receiver of the signal, if that remote receiver has detected a B1 error. In that case, the B1 error mask is copied and sent back as the M1 byte.

0x800030, 810088, 820088, 830088 Loss of Frame Count

Access / Notes: 32-bit read-only

0x800030 (Port 0): STRATIX5_REGXL8(STRATIX5_LOF_CNT, 0)
0x810088 (Port 1): STRATIX5_REGXL8(STRATIX5_LOF_CNT, 1)
0x820088 (Port 2): STRATIX5_REGXL8(STRATIX5_LOF_CNT, 2)
0x830088 (Port 3): STRATIX5_REGXL8(STRATIX5_LOF_CNT, 3)

Bit	Access	Name	Description
31–0	R only	[no name]	The number of times framing was lost since the counter was last reset. This number equals the number of times bit 15 (S5_RXFRM_FRM_LCKD) in register 0x800000, 810000, 820000, 830000 Receive Framer Status and Control has gone clear. Framing is lost when four consecutive bad framing patterns are detected.

0x800034, 810034, 820034, 830034 Pattern Error Count

Access / Notes: 32-bit read-only

0x800034 (Port 0): STRATIX5_REGXL8(STRATIX5_PAT_ERR_CNT, 0)
0x810034 (Port 1): STRATIX5_REGXL8(STRATIX5_PAT_ERR_CNT, 1)
0x820034 (Port 2): STRATIX5_REGXL8(STRATIX5_PAT_ERR_CNT, 2)
0x830034 (Port 3): STRATIX5_REGXL8(STRATIX5_PAT_ERR_CNT, 3)

Bit	Access	Name	Description
31–0	R only	[no name]	The number of times that the framing pattern was not correct, after data has been in frame. Because framing is not lost until the framing pattern has been incorrect four consecutive times, an incorrect framing pattern does not necessarily mean that framing was lost.

0x80003C, 81003C, 82003C, 83003C Demux Bitmask

Access / Notes: 32-bit read-only

Addresses and writes a 192-bit mask which can be used to select timeslots from an SDH / SONET frame. Writing a 1 to a bit will disable that bit's timeslot.

0x80003C (Port 0): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK, 0)
0x81003C (Port 1): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK, 1)
0x82003C (Port 2): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK, 2)
0x83003C (Port 3): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK, 3)

Bit	Access	Name	Description
31	RW	[no name]	Set to write data in bits 7–0 to address in bits 12–8.
30–13	–	–	Reserved.
12–8	RW	[no name]	Address for a 4-bit or 8-bit section of the mask.
7–0	RW	[no name]	Data to be written to the mask. For OC3 / STM1, OC12 / STM4, and OC48 / STM16, only four bits are addressed per write; for OC192 / STM64, eight bits are addressed per write.

STM1

The mask is written 4 bits at a time; only the first 3 bits [0–2] of the mask are used.

Example: To select AU-3(1), the first AU-3, use the pdb command...

: wm132 80003C 80000003

STM4

The mask is written 4 bits at a time; only the first 12 bits [0–11] of the mask are used.

Example: To select AU-4(1,0), the first STM1, use the pdb commands...

: wm132 80003C 80000007
: wm132 80003C 80000107
: wm132 80003C 80000207

...or to select AU-3(1,1), the first AU-3, use the commands...

: wm132 80003C 80000007
: wm132 80003C 8000010F
: wm132 80003C 8000020F

STM16

The mask is written 4 bits at a time; only the first 48 bits [0–47] of the mask are used.

Example: To select AU-4(1,1,0), the first STM1, use the pdb commands...

: wm132 80003C 80000007
: wm132 80003C 8000010F
: wm132 80003C 8000020F
: wm132 80003C 8000030F
: wm132 80003C 80000407
: wm132 80003C 8000050F
: wm132 80003C 8000060F
: wm132 80003C 8000070F
: wm132 80003C 80000807
: wm132 80003C 8000090F
: wm132 80003C 80000A0F
: wm132 80003C 80000B0F

STM64

The mask is written 8 bits at a time; all 192 bits are used.

Example: To select AU-4(1,1,1,0), the first STM1, use the pdb commands...

: wm132 80003C 8000007F
: wm132 80003C 800001FF
: wm132 80003C 800002FF
: wm132 80003C 800003FF
: wm132 80003C 800004FF
: wm132 80003C 800005FF
: wm132 80003C 800006FF
: wm132 80003C 800007FF
: wm132 80003C 8000087F
: wm132 80003C 800009FF
: wm132 80003C 80000AFF
: wm132 80003C 80000BFF
: wm132 80003C 80000CFF
: wm132 80003C 80000DFF
: wm132 80003C 80000EFF
: wm132 80003C 80000FFF
: wm132 80003C 8000107F
: wm132 80003C 800011FF
: wm132 80003C 800012FF
: wm132 80003C 800013FF
: wm132 80003C 800014FF
: wm132 80003C 800015FF
: wm132 80003C 800016FF
: wm132 80003C 800017FF

0x800040, 810040, 820040, 830040 Demux Bitmask Readback

Access / Notes: 32-bit read-only

0x800040 (Port 0): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK_RDBCK, 0)
0x810040 (Port 1): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK_RDBCK, 1)
0x820040 (Port 2): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK_RDBCK, 2)
0x830040 (Port 3): STRATIX5_REGXL8(STRATIX5_DEMUX_BITMASK_RDBCK, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7–0	R only	[no name]	Data from the section of the mask addressed in STRATIX5_DEMUX_BITMASK. For OC3 / STM1, OC12 / STM4, and OC48 / STM16, only bits 3–0 are valid.

0x800060, 810060, 820060, 830060 Detailed Port Status

Access / Notes: 32-bit read-only

0x800060 (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_STAT2, 0)
0x810060 (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_STAT2, 1)
0x820060 (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_STAT2, 2)
0x830060 (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_STAT2, 3)

Bit	Access	Name	Description
31–2	–	–	Reserved.
1	R only	[no name]	Lane 0 transceiver clock and data recovery (CDR) is locked to data.
0	R only	[no name]	Lane 0 transceiver clock and data recovery (CDR) is locked to reference clock.

0x800064, 810064, 820064, 830064 Transceiver Reconfiguration Address and Control

Access / Notes: 32-bit read-write

0x800064 (Port 0): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_ADDR, 0)
0x810064 (Port 1): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_ADDR, 1)
0x820064 (Port 2): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_ADDR, 2)
0x830064 (Port 3): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_ADDR, 3)

Bit	Access	Name	Description
31–19	–	–	Reserved.
18	RW	[no name]	Caution: This bit affects all ports. Set to reset the entire FPGA transceiver reconfiguration interface.
17	R only	[no name]	Set when the transceiver reconfiguration interface is busy.
16	RW	[no name]	Set to reset the port's transceiver.
15–0	RW	[no name]	Reconfiguration register address.

0x800068, 810068, 820068, 830068 Transceiver Reconfiguration Write Data

Access / Notes: 32-bit read-write

0x800068 (Port 0): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_WDATA, 0)
0x810068 (Port 1): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_WDATA, 1)
0x820068 (Port 2): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_WDATA, 2)
0x830068 (Port 3): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_WDATA, 3)

Bit	Access	Name	Description
31–0	RW	[no name]	Reconfiguration interface write data.

0x80006C, 81006C, 82006C, 83006C Transceiver Reconfiguration Read Data

Access / Notes: 32-bit read-only

0x80006C (Port 0): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_RDATA, 0)
0x81006C (Port 1): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_RDATA, 1)
0x82006C (Port 2): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_RDATA, 2)
0x83006C (Port 3): STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_RDATA, 3)

Bit	Access	Name	Description
31–0	R only	[no name]	Reconfiguration interface read data.

0x800074, 810074, 820074, 830074 Frequency Counter Enable

Access / Notes: 32-bit read-write

0x800074 (Port 0): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_EN, 0)
0x810074 (Port 1): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_EN, 1)
0x820074 (Port 2): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_EN, 2)
0x830074 (Port 3): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_EN, 3)

Bit	Access	Name	Description
31–1	–	–	Reserved.
0	RW	[no name]	Set to enable frequency counter.

0x800078, 810078, 820078, 830078 Receive Frequency Counter

Access / Notes: 32-bit read-only

0x800078 (Port 0): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_RX, 0)
0x810078 (Port 1): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_RX, 1)
0x820078 (Port 2): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_RX, 2)
0x830078 (Port 3): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_RX, 3)

Bit	Access	Name	Description
31–24	–	–	Reserved.
23–0	R only	[no name]	Receive frequency counter value.

0x80007C, 81007C, 82007C, 83007C Transmit Frequency Counter

Access / Notes: 32-bit read-only
0x80007C (Port 0): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_TX, 0)
0x81007C (Port 1): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_TX, 1)
0x82007C (Port 2): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_TX, 2)
0x83007C (Port 3): STRATIX5_REGXL8(STRATIX5_FREQ_CNT_TX, 3)

Bit	Access	Name	Description
31–24	–	–	Reserved.
23–0	R only	[no name]	Transmit frequency counter value.

0x800080, 810080, 820080, 830080 PRBS Mode

Access / Notes: 32-bit read-only
0x800080 (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_MODE, 0)
0x810080 (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_MODE, 1)
0x820080 (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_MODE, 2)
0x830080 (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_MODE, 3)

Bit	Access	Name	Description
31–8	–	–	Reserved.
7–0	RW	[no name]	PRBS mode.

0x800084, 810084, 820084, 830084 PRBS Control 0

Access / Notes: 32-bit read-write
0x800084 (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL0, 0)
0x810084 (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL0, 1)
0x820084 (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL0, 2)
0x830084 (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL0, 3)

Bit	Access	Name	Description
31	–	–	Reserved.
30	R only	[no name]	Lane 1 transmit PRBS realtime error.
29	R only	[no name]	Lane 1 transmit PRBS latched error.
28	R only	[no name]	Lane 1 transmit PRBS synchronized.
27–26	–	–	Reserved.
25	RW	[no name]	Lane 1 transmit PRBS check enable.
24	RW	[no name]	Lane 1 transmit PRBS generate enable.
23	–	–	Reserved.
22	R only	[no name]	Lane 1 receive PRBS realtime error.
21	R only	[no name]	Lane 1 receive PRBS latched error.
20	R only	[no name]	Lane 1 receive PRBS synchronized.
19–18	–	–	Reserved.
17	RW	[no name]	Lane 1 receive PRBS check enable.
16	RW	[no name]	Lane 1 receive PRBS generate enable.
15	–	–	Reserved.
14	R only	[no name]	Lane 0 transmit PRBS realtime error.

13	R only	[no name]	Lane 0 transmit PRBS latched error.
12	R only	[no name]	Lane 0 transmit PRBS synchronized.
11–10	–	–	Reserved.
9	RW	[no name]	Lane 0 transmit PRBS check enable.
8	RW	[no name]	Lane 0 transmit PRBS generate enable.
7	–	–	Reserved.
6	R only	[no name]	Lane 0 receive PRBS realtime error.
5	R only	[no name]	Lane 0 receive PRBS latched error.
4	R only	[no name]	Lane 0 receive PRBS synchronized.
3–2	–	–	Reserved.
1	RW	[no name]	Lane 0 receive PRBS check enable.
0	RW	[no name]	Lane 0 receive PRBS generate enable.

0x800088, 810088, 820088, 830088 PRBS Control 1

Access / Notes: 32-bit read-write

0x800088 (Port 0): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL1, 0)
0x810088 (Port 1): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL1, 1)
0x820088 (Port 2): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL1, 2)
0x830088 (Port 3): STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL1, 3)

Bit	Access	Name	Description
31	–	–	Reserved.
30	R only	[no name]	Lane 3 transmit PRBS realtime error.
29	R only	[no name]	Lane 3 transmit PRBS latched error.
28	R only	[no name]	Lane 3 transmit PRBS synchronized.
27–26	–	–	Reserved.
25	RW	[no name]	Lane 3 transmit PRBS check enable.
24	RW	[no name]	Lane 3 transmit PRBS generate enable.
23	–	–	Reserved.
22	R only	[no name]	Lane 3 receive PRBS realtime error.
21	R only	[no name]	Lane 3 receive PRBS latched error.
20	R only	[no name]	Lane 3 receive PRBS synchronized.
19–18	–	–	Reserved.
17	RW	[no name]	Lane 3 receive PRBS check enable.
16	RW	[no name]	Lane 3 receive PRBS generate enable.
15	–	–	Reserved.
14	R only	[no name]	Lane 2 transmit PRBS realtime error.
13	R only	[no name]	Lane 2 transmit PRBS latched error.
12	R only	[no name]	Lane 2 transmit PRBS synchronized..
11–10	–	–	Reserved.
9	RW	[no name]	Lane 2 transmit PRBS check enable.
8	RW	[no name]	Lane 2 transmit PRBS generate enable.
7	–	–	Reserved.
6	R only	[no name]	Lane 2 receive PRBS realtime error.
5	R only	[no name]	Lane 2 receive PRBS latched error.

4	R only	[no name]	Lane 2 receive PRBS synchronized.
3–2	–	–	Reserved.
1	RW	[no name]	Lane 2 receive PRBS check enable.
0	RW	[no name]	Lane 2 receive PRBS generate enable.

0x80008C, 81008C, 82008C, 83008C PRBS Control 2 [Reserved]

0x800090, 810090, 820090, 830090 PRBS Control 3 [Reserved]

0x800094, 810094, 820094, 830094 PRBS Control 4 [Reserved]

Registers, Port: Port 4 (QSFP)

0xA0–0xA7 Indirect

0xA0 QSFP Configuration and Status

		Access / Notes:	8-bit read-write / STRATIX5_REGXL8(STRATIX5_OPT_XCVR, 4)
Bit	**Access**	**Bit name**	**Description**
7	–	–	Reserved.
6	R only	[no name]	When set, indicates that the QSFP is asserting an interrupt.
5	R only	[no name]	When set, indicates that the QSFP is connected and detected.
4	–	–	Reserved.
3	–	–	Reserved.
2	RW	[no name]	Set to enable low power mode.
1	RW	[no name]	Set to enable transceiver.
0	–	–	Reserved.

0xA1 Port Enable

		Access / Notes:	8-bit read-write / STRATIX5_REGXL8(STRATIX5_PORT_CTRL, 4)
Bit	**Access**	**Name**	**Description**
7–3	–	–	Reserved.
2	RW	[no name]	Set to enable PLL1 (not used).
1	RW	[no name]	Set to enable PLL0 (not used).
0	RW	[no name]	Set to enable the LIU (not used).

0xA2 Port Status

		Access / Notes:	8-bit read-only / STRATIX5_REGXL8(STRATIX5_PORT_STAT, 4)
Bit	**Access**	**Name**	**Description**
7	–	–	Reserved.
6	R only	[no name]	When set, indicates the transceiver reconfiguration is in progress.
5	–	–	Reserved.
4	R only	[no name]	When set, indicates the transceiver transmit PLL0 is locked.
3	R only	[no name]	When set, indicates the transceiver CDR is locked to data.
2	R only	[no name]	When set, indicates the transceiver CDR is locked to reference clock.
1	R only	[no name]	When set, indicates the transceiver is ready to receive.
0	R only	[no name]	When set, indicates the transceiver is ready to transmit.

0xA3 QSFP Status 2 [Reserved]

0xA7 Port Information

		Access / Notes:	8-bit read-only / STRATIX5_REGXL8(STRATIX5_PORT_INFO, 4)
Bit	**Access**	**Name**	**Description**
7–4	R only	[no name]	Port type (QSFP=1).
3–0	R only	[no name]	Port number.

Registers, Port: Port 4 (QSFP/+)

0x840010–0x840098 BAR1 Memory-Mapped

0x840010 Synchronization Control

		Access / Notes:	32-bit read-write / STRATIX5_REGXL8(STRATIX5_PSYNC_CTRL, 4)
Bit	**Access**	**Name**	**Description**
31–16	–	–	Reserved.
15	RW	STRATIX5_ TXTRIG_ARM	Set to arm transmit trigger.
14	–	–	Reserved.
13–12	RW	[no name]	Select when DDR3 FIFO transmit will start: 0 = ignore 1 = when FIFO is 50% full 2 = when FIFO is 75% full 3 = when FIFO is 100% full The transmit logic waits to transmit until the selected threshold is reached.
11–10	–	–	Reserved.
9–8	RW	[no name]	Select transmit trigger source: 0 = external 1 = internal
7	RW	STRATIX5_ RXTRIG_ARM	Set to arm receive trigger.
6–3	–	–	Reserved.
2	RW	[no name]	Set to disable wait for frame receive trigger mode.
1–0	RW	[no name]	Select receive trigger source: 0 = external 1 = internal

0x840014 Frame Count Control [Reserved]

0x840060 Detailed Port Status

		Access / Notes:	32-bit read-only / STRATIX5_REGXL8(STRATIX5_PORT_STAT2, 4)
Bit	**Access**	**Name**	**Description**
31–8	–	–	Reserved.
7	R only	[no name]	Lane 3 transceiver clock and data recovery (CDR) is locked to data.
6	R only	[no name]	Lane 3 transceiver clock and data recovery (CDR) is locked to reference clock.
5	R only	[no name]	Lane 2 transceiver clock and data recovery (CDR) is locked to data.
4	R only	[no name]	Lane 2 transceiver clock and data recovery (CDR) is locked to reference clock.

3	R only	[no name]	Lane 1 transceiver clock and data recovery (CDR) is locked to data.
2	R only	[no name]	Lane 1 transceiver clock and data recovery (CDR) is locked to reference clock.
1	R only	[no name]	Lane 0 transceiver clock and data recovery (CDR) is locked to data.
0	R only	[no name]	Lane 0 transceiver clock and data recovery (CDR) is locked to reference clock.

0x840064 Transceiver Reconfiguration Address and Control

		Access / Notes:	32-bit read-write **/** STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_ADDR, 4)
Bit	**Access**	**Name**	**Description**
31–19	–	–	Reserved.
18	RW	[no name]	Caution: This bit affects all ports. Set to reset the entire FPGA transceiver reconfiguration interface.
17	R only	[no name]	Set when the transceiver reconfiguration interface is busy.
16	RW	[no name]	Set to reset the port's transceiver.
15–0	RW	[no name]	Reconfiguration register address.

0x840068 Transceiver Reconfiguration Address and Control

		Access / Notes:	32-bit read-write **/** STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_WDATA, 4)
Bit	**Access**	**Name**	**Description**
31–0	RW	[no name]	Reconfigure interface write data.

0x84006C Transceiver Reconfiguration Address and Control

		Access / Notes:	32-bit read-only **/** STRATIX5_REGXL8(STRATIX5_XCVR_MGMT_RDATA, 4)
Bit	**Access**	**Name**	**Description**
31–0	R only	[no name]	Reconfigure interface read data.

0x840074 Frequency Counter Enable

		Access / Notes:	32-bit read-write **/** STRATIX5_REGXL8(STRATIX5_FREQ_CNT_EN, 4)
Bit	**Access**	**Name**	**Description**
31–1	–	–	Reserved.
0	RW	[no name]	Set to enable to frequency counter.

0x840078 Receive Frequency Counter

		Access / Notes:	32-bit read-only **/** STRATIX5_REGXL8(STRATIX5_FREQ_CNT_RX, 4)
Bit	**Access**	**Name**	**Description**
31–24	–	–	Reserved.
23–0	R only	[no name]	Receive frequency counter value.

0x84007C Transmit Frequency Counter

		Access / Notes:	32-bit read-only / STRATIX5_REGXL8(STRATIX5_FREQ_CNT_TX, 4)
Bit	**Access**	**Name**	**Description**
31–24	–	–	Reserved.
23–0	R only	[no name]	Transmit frequency counter value.

0x840080 PRBS Mode

		Access / Notes:	32-bit read-write / STRATIX5_REGXL8(STRATIX5_PORT_PRBS_MODE, 4)
Bit	**Access**	**Name**	**Description**
31–8	–	–	Reserved.
7–0	RW	[no name]	PRBS mode.

0x840084 PRBS Control 0

		Access / Notes:	32-bit read-write / STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL0, 4)
Bit	**Access**	**Name**	**Description**
31	–	–	Reserved.
30	R only	[no name]	Lane 1 transmit PRBS realtime error.
29	R only	[no name]	Lane 1 transmit PRBS latched error.
28	R only	[no name]	Lane 1 transmit PRBS synchronized.
27–26	–	–	Reserved.
25	RW	[no name]	Lane 1 transmit PRBS check enable.
24	RW	[no name]	Lane 1 transmit PRBS generate enable.
23	–	–	Reserved.
22	R only	[no name]	Lane 1 receive PRBS realtime error.
21	R only	[no name]	Lane 1 receive PRBS latched error.
20	R only	[no name]	Lane 1 receive PRBS synchronized.
19–18	–	–	Reserved.
17	RW	[no name]	Lane 1 receive PRBS check enable.
16	RW	[no name]	Lane 1 receive PRBS generate enable.
15	–	–	Reserved.
14	R only	[no name]	Lane 0 transmit PRBS realtime error.
13	R only	[no name]	Lane 0 transmit PRBS latched error.
12	R only	[no name]	Lane 0 transmit PRBS synchronized.
11–10	–	–	Reserved.
9	RW	[no name]	Lane 0 transmit PRBS check enable.
8	RW	[no name]	Lane 0 transmit PRBS generate enable.
7	–	–	Reserved.
6	R only	[no name]	Lane 0 receive PRBS realtime error.
5	R only	[no name]	Lane 0 receive PRBS latched error.

4	R only	[no name]	Lane 0 receive PRBS synchronized.
3–2	–	–	Reserved.
1	RW	[no name]	Lane 0 receive PRBS check enable.
0	RW	[no name]	Lane 0 receive PRBS generate enable.

0x840088 PRBS Control 1

		Access / Notes:	32-bit read-write **/** STRATIX5_REGXL8(STRATIX5_PORT_PRBS_CTRL1, 4)
Bit	**Access**	**Name**	**Description**
31	–	–	Reserved.
30	R only	[no name]	Lane 3 transmit PRBS realtime error.
29	R only	[no name]	Lane 3 transmit PRBS latched error.
28	R only	[no name]	Lane 3 transmit PRBS synchronization.
27–26	RW	[no name]	Reserved.
25	RW	[no name]	Lane 3 transmit PRBS check enable.
24	RW	[no name]	Lane 3 transmit PRBS generate enable.
23	–	–	Reserved.
22	R only	[no name]	Lane 3 receive PRBS realtime error.
21	R only	[no name]	Lane 3 receive PRBS latched error.
20	R only	[no name]	Lane 3 receive PRBS synchronization.
19–18	RW	[no name]	Reserved.
17	RW	[no name]	Lane 3 receive PRBS check enable.
16	RW	[no name]	Lane 3 receive PRBS generate enable.
15	–	–	Reserved.
14	R only	[no name]	Lane 2 transmit PRBS realtime error.
13	R only	[no name]	Lane 2 transmit PRBS latched error.
12	R only	[no name]	Lane 2 transmit PRBS synchronization.
11–10	RW	[no name]	Reserved.
9	RW	[no name]	Lane 2 transmit PRBS check enable.
8	RW	[no name]	Lane 2 transmit PRBS generate enable.
7	–	–	Reserved.
6	R only	[no name]	Lane 2 receive PRBS realtime error.
5	R only	[no name]	Lane 2 receive PRBS latched error.
4	R only	[no name]	Lane 2 receive PRBS synchronization.
3–2	–	–	Reserved.
1	RW	[no name]	Lane 2 receive PRBS check enable.
0	RW	[no name]	Lane 2 receive PRBS generate enable.

0x84008C PRBS Control 2 [Reserved]

0x840090 PRBS Control 3 [Reserved]

0x840094 PRBS Control 4 [Reserved]

Revision Log

Below is a history of modifications to this guide.

Date	By	Rev.	Pg(s)	Detail
20170104	PH,RH	0001	4	Corrected “www.edt.com/downloads/api” to “www.edt.com/api/”.
20140730	PH,SB,TL	0000	All	Created this new guide.