EAGLE HARBOR TECHNOLOGIES

User's Manual for Integrator Short Pulse ISP16

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EAGLE HARBOR TECHNOLOGIES

Specifications

Exceeding any of the Maximum Ratings and/or failing to follow any of the Warnings and/or Operating Instructions may result in damage to or failure of the integrator, or incorrect output signals.

Maximum continuous input voltage: 10 V[a]
Maximum pulse input voltage: 175 V[a]
Maximum output voltage: +/- 8 V[b]
Minimum output load: 50 Ω
Input resistance to ground: 50 kΩ[b]
Provided external AC-DC converters input power: 110-240VAC, 50-60 Hz, 1.5 A each

RC Time: 1 μs – 100 ms, custom set for each channel[b]
Droop: RC dependent, see figures
Drift: RC dependent, see figures
Calibration: +/- 10% for each channel[c]
Offset adjustment: < 5 mV

Common Mode Noise Rejection: < 1 mV/s (no effect detected) with 1 MHz +/- 20V
Channel - Channel Crosstalk: < 1 mV effect (no effect detected) when adjacent channel undergoes 5V excursion

Input impedance: 100 Ohms[b]
Input filtering to ground: none[b]
Input voltage clamp: none[b]
Input Connectors: RJ45, BNC[b]
Output Connectors: RJ45, BNC[b]

[a] The input has a 1 W 100 Ω termination resistor. The input voltage can exceed 10 V for short periods or at a low enough duty cycle so that the 1 W power rating of the resistor is not exceeded. The RJ45 input connector is limited to +/- 175V, so never exceed this input voltage.
[b] Integrators with different values, ranges, connectors, options are available.
[c] Precision factory calibration available. These can be corrected for in post processing.

Related Equipment:
If longer operation and/or higher gain operation and/or higher effective bit depth is required, then EHT has the long pulse integrator (ILP8) that can run continuously, and meets ITER stability requirements

Warnings:
Integrator Chassis does not tie to earth ground through input power connectors. See discussion below.

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System Description

Overview:

The ISP16-1000 is a 16 channel analog integrator. Each channel has its own RJ45 and BNC inputs and RJ45 and BNC outputs. All channels are triggered simultaneously and are controlled by the input "Enable" BNC.

When the Enable input is in the low state, all channels are in reset mode, which automatically zeroes their outputs. The integrators need about 1 sec prior to being gated on, with no input signal applied, to properly zero (the longer RC time channels need a longer zeroing period, up to 10 seconds). When the Enable input is in the high state, all channels are in the active mode, and their output will correspond to the time-integral of the input. Specifically, the output of an ideal integrator is given by:

$$V_{OUT} = \frac{1}{RC}\int_0^T V(t)dt$$

RC is the integration time constant of that channel. The RC time constant can be independently set for each channel with a physical resistor.

Integrators have several types of error on the output that must be considered: drift, droop, offset, and calibration.

Drift is an output voltage that strays away from zero over time, even when the input voltage is held at zero. It results from phenomena such as contact potentials, thermal gradients, inherent instabilities of operational amplifiers, etc. All analog integrators suffer from drift error to some extent and the goal with integrator design is to ensure that drift error is small compared to the signal of interest over the relevant timescale. Generally, drift error in analog integrators results from a runaway instability of some sort, meaning that drift becomes exponentially worse over time, limiting the maximum time that an integrator can run before the drift becomes excessive. In the case of the ISP16, the drift is dependent on the RC value, presented in a graph in the data section. In general, drift error is a random process that can not be corrected for in post processing.

Droop is a tendency of the output to droop back towards zero after integrating a real input signal. An ideal integrator would hold its output voltage constant forever after integrating a specified input signal, whereas a real integrator's output will droop. The droop of the ISP16 is dependent on the RC value, presented in a graph in the data section. In general, droop can be corrected for in post-processing.

Offset error is simply a DC offset in the output of an integrator. In the case of the ISP16, this has been adjusted to be less than 2 mV for each channel, through use of an internal pot. This offset may change slightly with temperature. The offset error can be fully corrected for in post processing.

Calibration error is a scaling factor in the output voltage equation above. This can be considered simply an error in the RC time constant. For example, a 10 ms RC integrator will have an output of 1 V after applying a 1 V input to it for 10 ms. If the calibration is only good to within +/-10%, then the output could be anywhere from 0.9 V to 1.1 V. The calibration error can be fully corrected for in post processing, as long as the user has a reliable calibration signal.

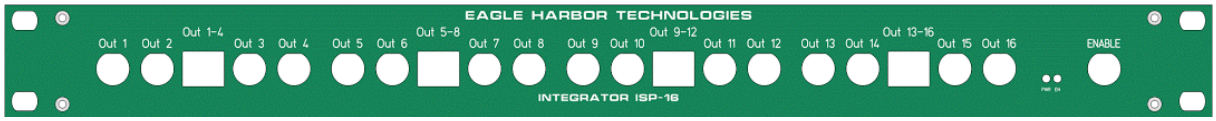

Figure 1. ISP16 Front Panel

The front panel (Figure 1) of the ISP16 has a separate BNC output for each channel and RJ45 outputs, each of which contains 4 channels. At the right of the front panel, there are:

1) PWR ON LED
   The AC ON LED is on whenever the ISP16 is plugged into power and the switch on the back panel is on.

2) EN LED
   The EN (enable) LED is on whenever a high signal (5V) is given to the ENABLE input. If the LED is on, that means all integrator channels are in active mode.

3) ENABLE INPUT
   The ENABLE input is used to trigger the integrator channels to active mode. The device used to control the ENABLE input must be able to drive a 50 Ω load to 5 VDC.

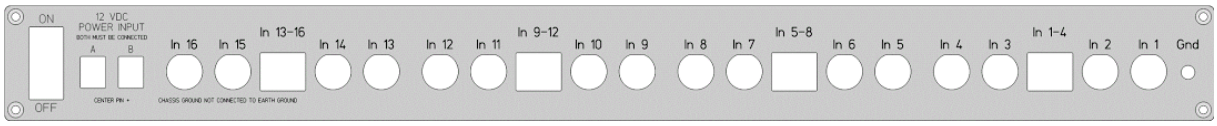

Figure 2. ISP16 Back Panel

The back panel (Figure 2) of the ISP16 has a separate BNC input for each channel and RJ45 inputs, each of which contains 4 channels. Additionally, the back panel contains the ON/OFF power switch, and two coaxial input power connectors. The two included 12V power supplies must be connected into both of the power connectors (A and B). Always plug in both connectors, and never attempt to turn on or operate the integrator without both connectors being plugged in.

RJ45 Channel Mapping

Each RJ45 input on the back panel and output on the front panel connectivity to 4 channels, as labeled on the front and back panels. The channel mapping matches the T568A standard. Each differential input signal comes in on one set of individually shielded twisted pair. The channel mapping is illustrated in Figure 3.

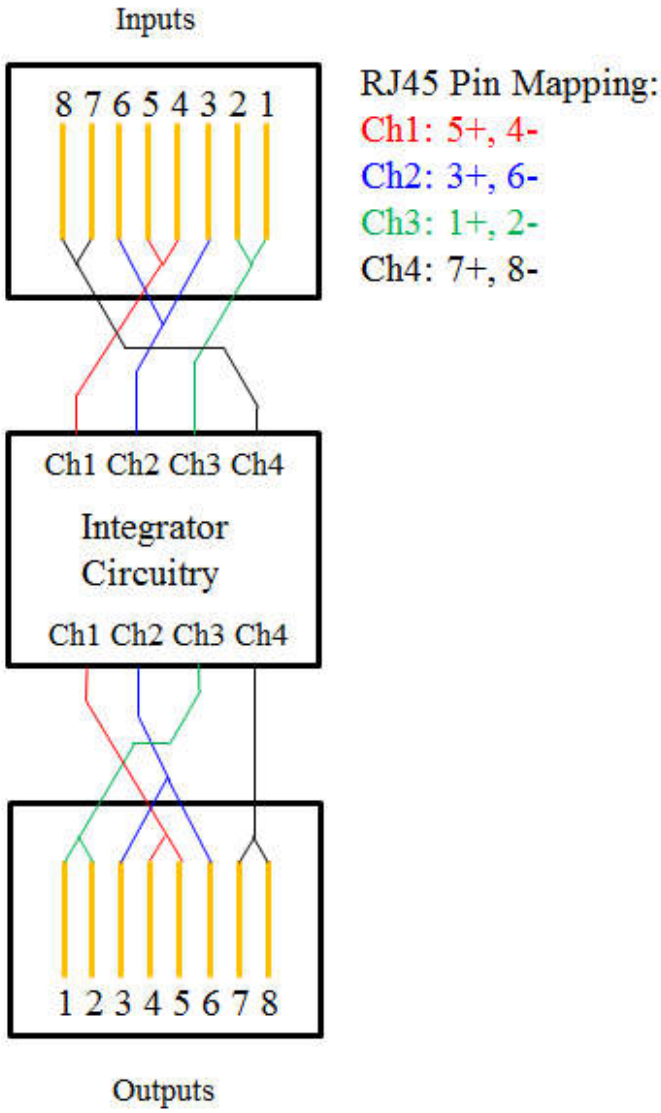

Figure 3. ISP16 RJ45 Connector Pin out Diagram

This repeats for each RJ45 connector.

Customization

The ISP16 integrator is available with a wide range of RC time constants, where each channel can be individually set. Typical RC times range from 1 μs to 100 ms, though the integrators have been operated with RC values outside this range as well. Selection of a small RC value is typically done when a very high gain is desired, and for short pulse experiments. Many other features of the ISP16 can be customized as well, including input and output connectorization and input terminations.

Channel-by-Channel Custom RC Times

This unit was customized with the following RC times:

33 μs – All Channels

Performance Data

Typical Performance

Testing for various inputs was conducted to make sure the integrator output was as expected. In Figures 4 and 5, short (~10 µs) and long (~50 ms) square wave signals (blue) were input into the integrator, respectively, resulting in the linear ramps shown (purple).

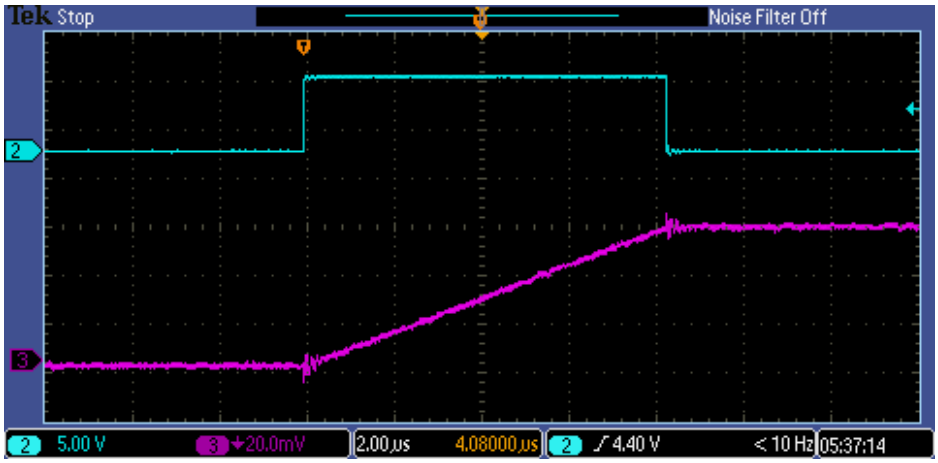

Figure 4. 10 µs Ramp

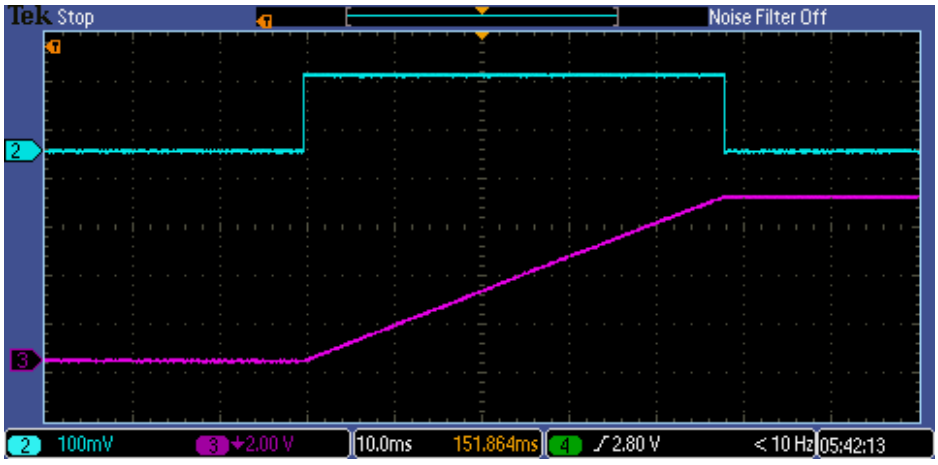

Figure 5. 50 ms Ramp

The next example waveform in Figure 6 was generated by connecting a magnetic pickup coil into the integrator input, and simply placing a magnet into the coil, waiting a brief time, and then pulling the magnet back out. As expected, the signal returns back to zero.

Figure 7 demonstrates both low and higher frequency performance of the integrator. The 6 s long main signal was generated with a magnetic pickup loop (as in Figure 11), with the high frequency signal shown in the blow-up view injected through a transformer-coupled function generator. Note that the integrator simultaneously fully resolves both signals. The higher

frequency signal shown is for demonstration only and is still not at the maximum frequency of the integrator.

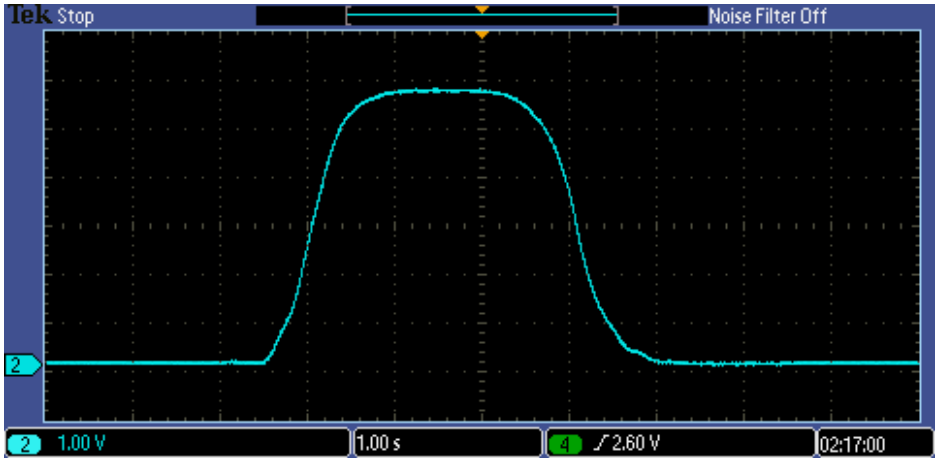

Figure 6. Magnetic Pickup Loop Signal

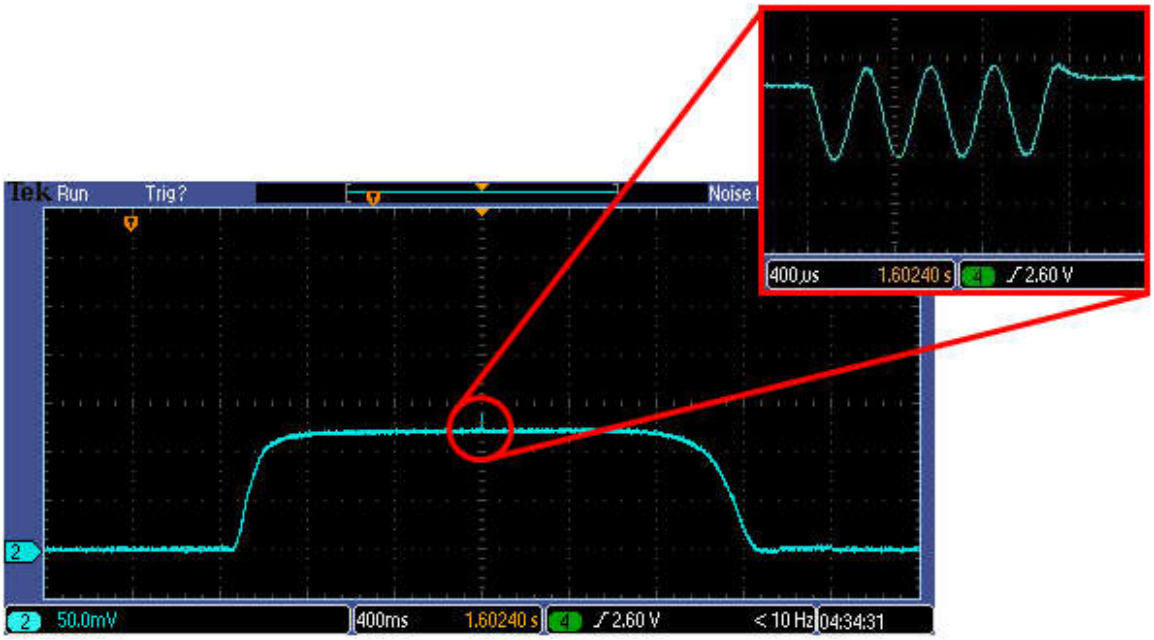

Figure 7. Frequency Range Demonstration

Frequency Response

The maximum frequency of an input signal that can be accurately integrated in terms of both gain and phase on the output is approximately 1 MHz.

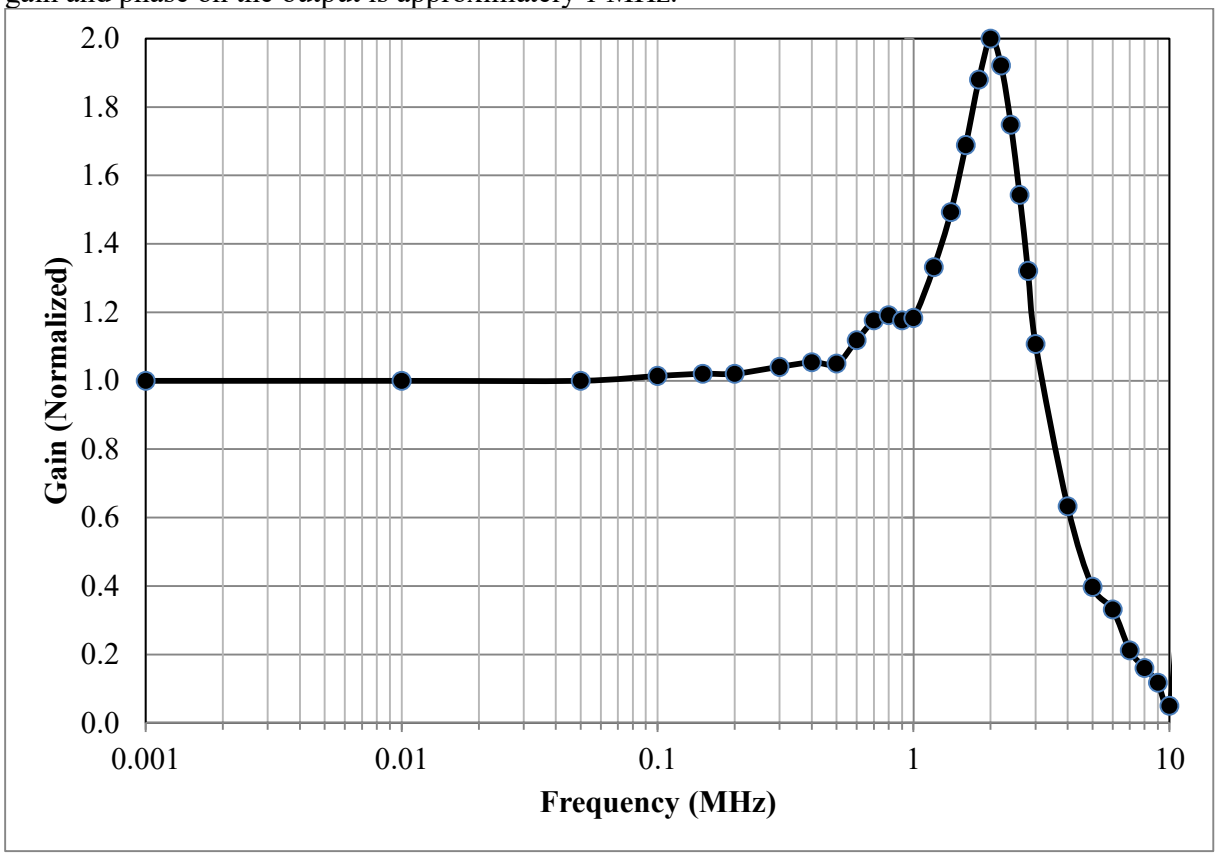

Figure 8. Frequency Response

Faster signals can still be integrated but may include a phase lag as well as incorrect gain and settling/overshoot features. For example, the waveform below is of a 200 ns input square wave with a fast rise and fall (frequency components up to ~15 MHz) into a 500 ns RC time integrator:

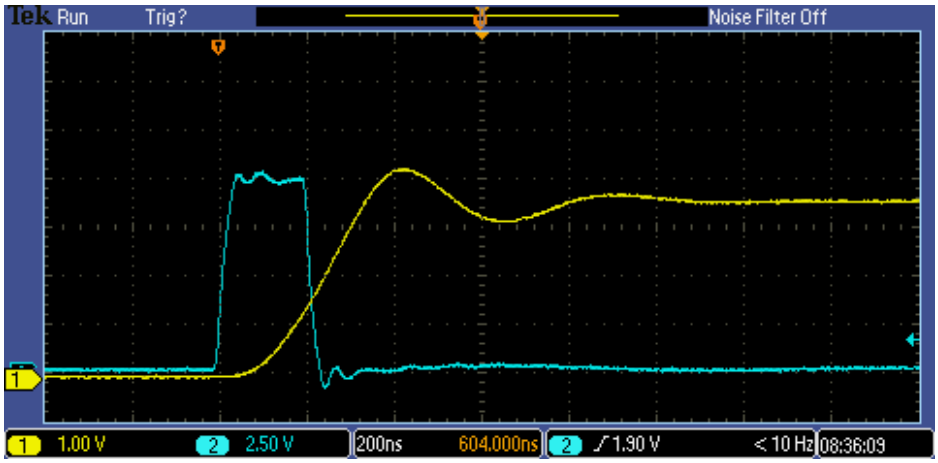

Figure 9. Fast Waveform Response

Droop Characteristics

The droop is dependent on the RC time. The droop rate is approximately inversely proportional to the RC time.

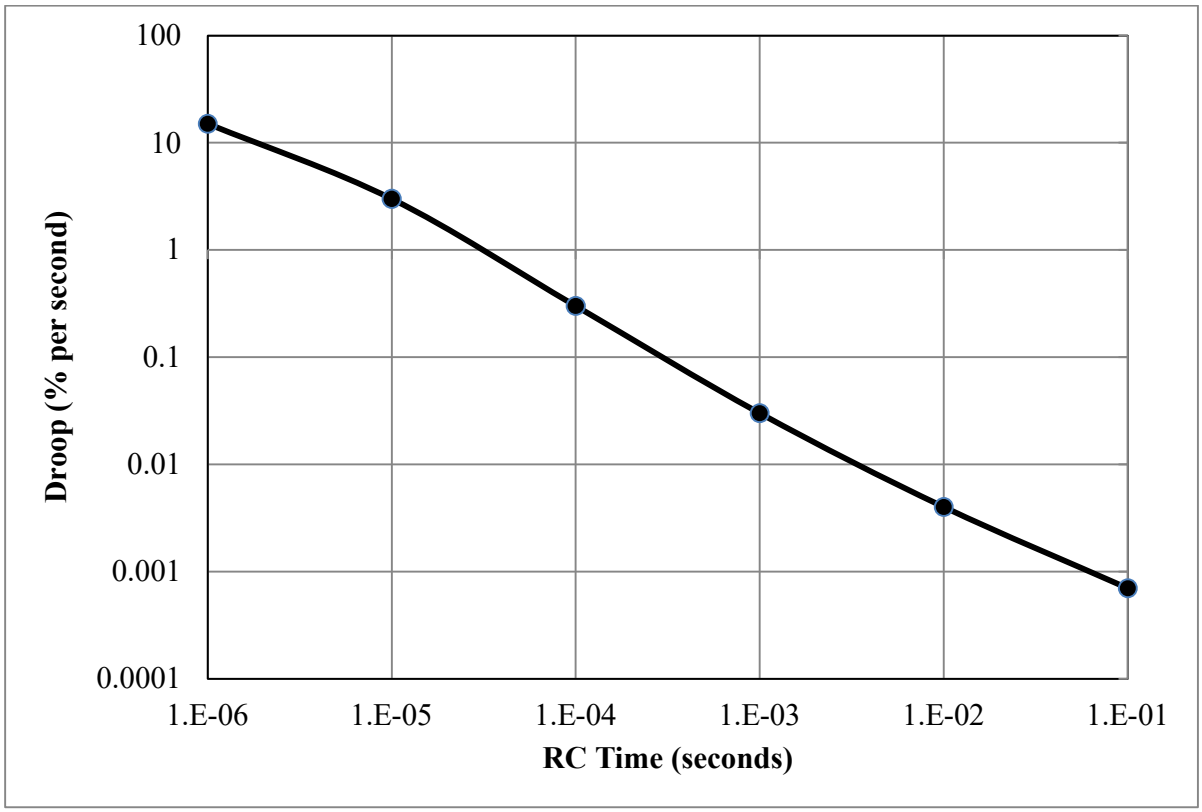

Figure 10. Droop vs RC Time

The droop was measured by integrating a large signal and then letting the integrator remain on for a long time until the droop became measurable. For example, here is the droop waveform of the 1 ms integrator, gated on for 100s:

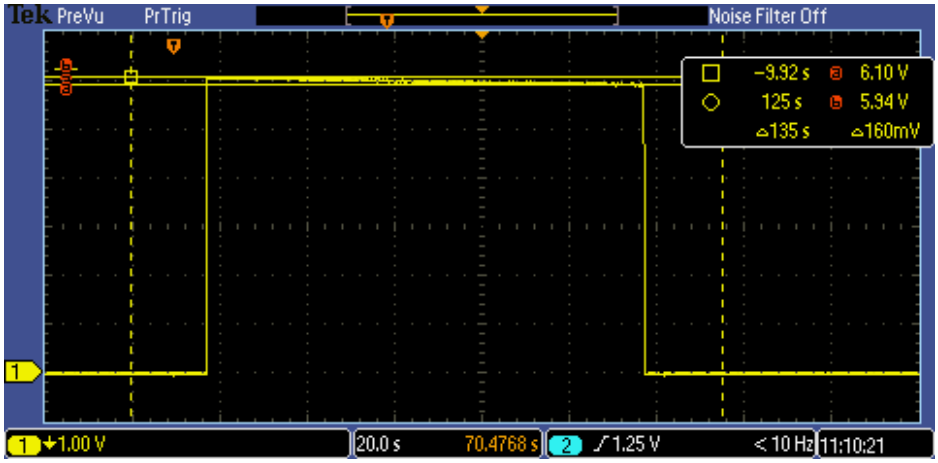

Figure 11. Droop Test Waveform

Drift Characteristics

Drifts were measured by looking at the typical random drift of all channels at any particular RC time and picking a characteristic upper bound on their drift. For example, here are typical drifts from a set of 4 different 10µs RC channels, being gated on for 1 second and then being allowed to reset for 1 second, and repeating several times. The upper bound in this case is characterized as 5 mV of drift although most instances of the drift fall well below that.

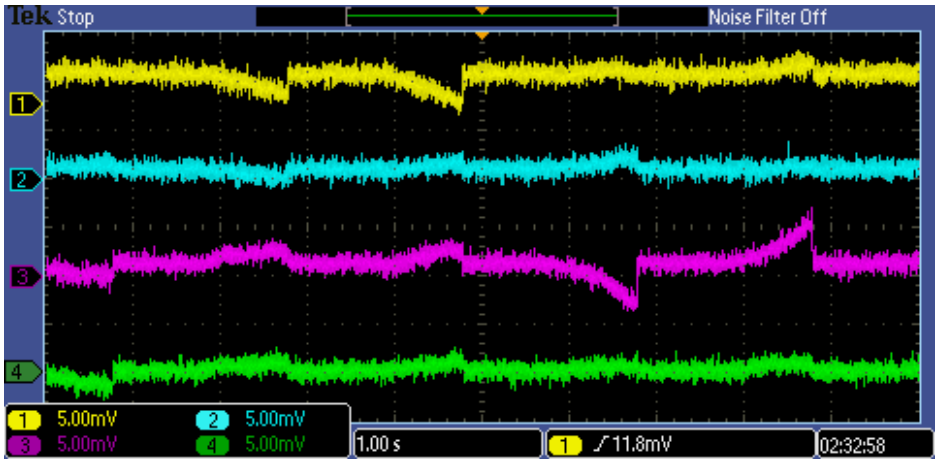

Figure 13. Drift Waveforms

The absolute value of the drift naturally decreases as the RC time constant increases:

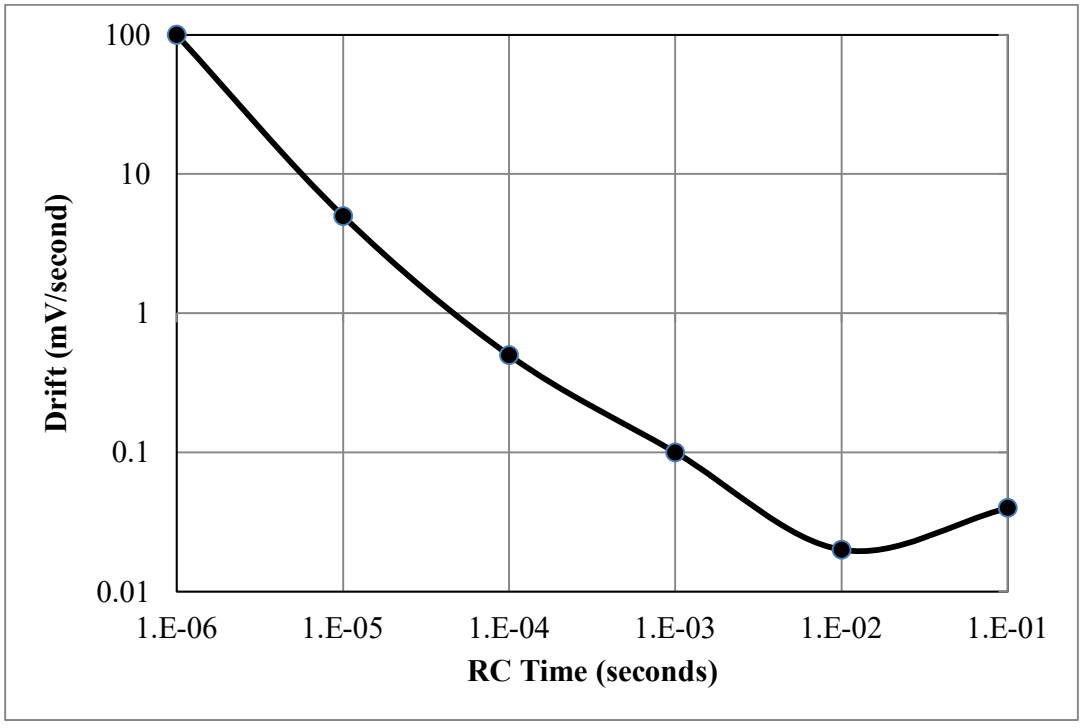

Figure 13. Drift vs RC Time

The performance of an integrator can be described in terms of a figure of merit, F = ΔV*RC/T, where ΔV is the drift, RC is the RC time of the integrator, and T is the time period over which the drift occurs. The above data can be presented in this form. The 100 ms figure of merit is out of line with the rest because the integrator has yet to be fully optimized at that RC time.

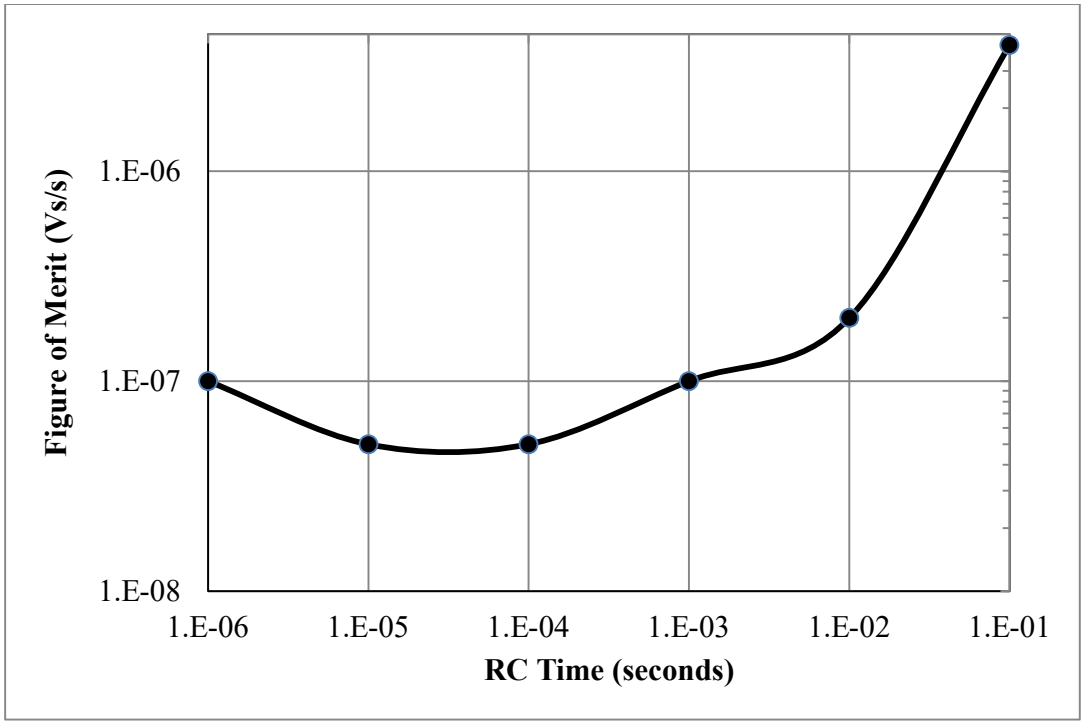

Figure 14. Figure of Merit vs RC Time

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Operating Instructions

Operation

Operation of the ISP16 is relatively straightforward. Attach inputs to the input connectors on the back. Attach outputs to the output connectors on the front, going into the user's DAQ system or oscilloscope.

Gate the integrator on (at the EN input) when (or preferably just before) a signal of interest is to be integrated. Use a 5V signal capable of driving 50 Ohms to gate the integrator on.

Note:

1) The integrators need about 1 sec prior to being gated on, with no input signal applied, to properly zero (for the 10ms and 100ms channels to properly zero, allow 10s of time prior to being gated on). If some signal is applied, the result will be an output that has a large linear drift to it. This linear drift can be removed through data post processing.

2) Do not exceed 5 VDC into the EN gate input.

3) If not gated on, the integrator will still appear to integrate large/fast signals, though these signals will exhibit large droop. This is the result of internal circuitry trying to zero the output while the integrator is in reset mode.

Interfacing and Shielding

The ISP16 has 16 separate individual inputs, one for each channel. The channels are bundled into groups of 4, each associated with an RJ45 input and output. The signals should be brought in through Cat 6e/7 cables, which have independent electrostatic shielding and where the two signal leads for each channel are individually shielded twisted pairs. This style of cable maintains the differential input of the integrator, which is important for optimal results. The BNC inputs can also be used, however, due to the non-differential nature of BNC cables, this may cause a degradation in integrator performance.

Care should be taken to maintain the differential nature and electrostatic shielding of the input signal as far as possible, ideally right up to (and over) the magnetic pickup loop being used with that channel. Sections of un-shielded and/or un-twisted wire on the input will allow noise to enter the system.

Calibration Testing

Prior to use in an experimental setting, the user should verify the calibration of the integrator, in regards to both DC offset and calibration error.

To check for DC offset, simply power the integrator on, do not connect any inputs, do not turn on the ENABLE input, and look at the output voltage of each channel with an oscilloscope or DAQ. The output voltage of each channel should be 0 V +/- 5 mV. If the DC offset voltage

exceeds +/- 20 mV, internal pots should be adjusted to bring the offset back under +/- 5 mV. Contact EHT prior to making this adjustment for detailed instructions.

Next, the user should look at the calibration of each channel relative to the input signal. The user should input a specified voltage signal for a specific amount of time into the integrator and look at the output into the DAQ. An example of such an input square wave is shown in the blue in Figure 15. The purple trace is the resulting output. The ISP16 integrates the square wave input and outputs a linear ramp.

An input square wave of voltage V_{in} for duration T should produce a linearly ramping output voltage, ending with the final value of $V_{out} = V_{in}T/RC$. V_{out} may vary by a few % from this value due to variation in precise values of resistors and capacitors used in the integrator, etc. Production units can be precisely calibrated at the factory if desired.

The user should record the overall calibration value for each channel and use it to correct the integrator's output data.

When performing calibration testing, the user should take care to ensure that whatever system is used to input signals into the integrator does not have a slight DC offset, as many standardly used signal/pulse generators typically do. A small DC offset in the input voltage will be integrated as a real input signal by the integrator. Getting rid of a DC offset coming out of a signal generator can often be achieved by transformer coupling the signal, though than transformer droop can become an issue. Other solutions involve using a signal generator that allows the DC offset to be precisely tuned so it can be dialed to zero, or using a photodiode to optically couple in a signal. These integrators are very sensitive, and readily integrate input DC offset signals.

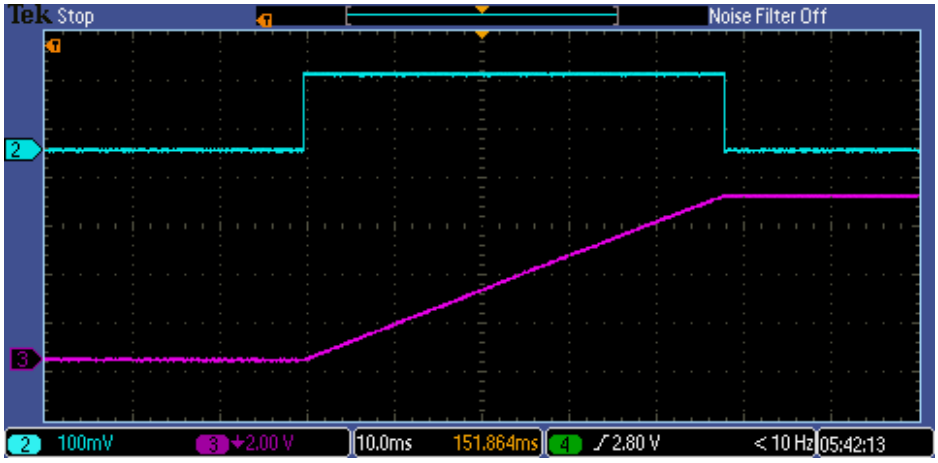

Figure 15. Input Square Wave (Blue), Integrator Output Ramp (Purple)

Grounding:

It is a feature of the ISP16 that the chassis is not tied to the input power ground. The user may tie the chassis to the rack that the ISP is mounted in, or to the input of a DAQ that the ISP16 is being used with. Always avoid creating ground loops when using the ISP16. Ideally, the chassis

would only be grounded at the DAQ, and the DAQ would have differential inputs. In addition, all input signals would be differential with no ground connections, and have isolated electrostatic shields that only ground at the integrator chassis. If the input signals are single sided, there is a real possibility that the integrator will respond to induced ground currents.

One effect of ground loops between the ISP16 and the DAQ can be a perceived crosstalk between the channels. Consider a voltage V_{sig} being input into the DAQ along a BNC cable from the ISP16, as shown in Figure 16. If the BNC cable is terminated with a resistance R_T = 50 Ω, then a fairly high current I = V_{sig} / 50 Ω will flow, and must then return back to the integrator through the ground shield of the BNC cable. The BNC cable has some real resistance R. If a second channel is also connected through a BNC cable, then half the current will flow back through that cable's ground shield, and will produce an offset voltage V_{off} = I/2 × R.

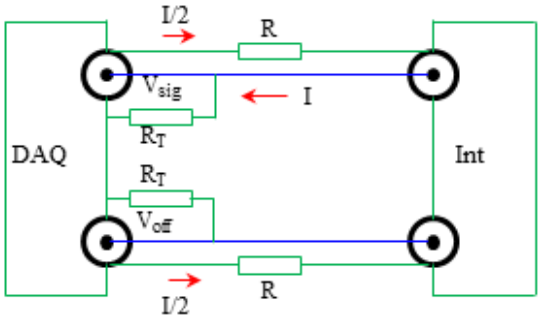

Figure 16. Ground Loop Resistance Issues

This effect is shown in Figure 17, where a 7 V signal on one channel (purple) causes a ~2 mV error on another channel (yellow). The perceived crosstalk can be reduced by increasing the value of the termination resistor R_T, which will reduce the current that flows and therefore the error voltage. The perceived crosstalk can also be reduced by minimizing the resistance of the cables connecting the integrator to the DAQ (i.e. by keeping the cables short).

However, the optimal solution is to use a DAQ with differential inputs that do not tie to ground, thus keeping each channel isolated from all others, avoiding the issue of currents returning through the ground shields of other channels. In Figure 18, the results using a differential probe are shown. Notice that the perceived crosstalk has been eliminated. No real crosstalk is detectable.

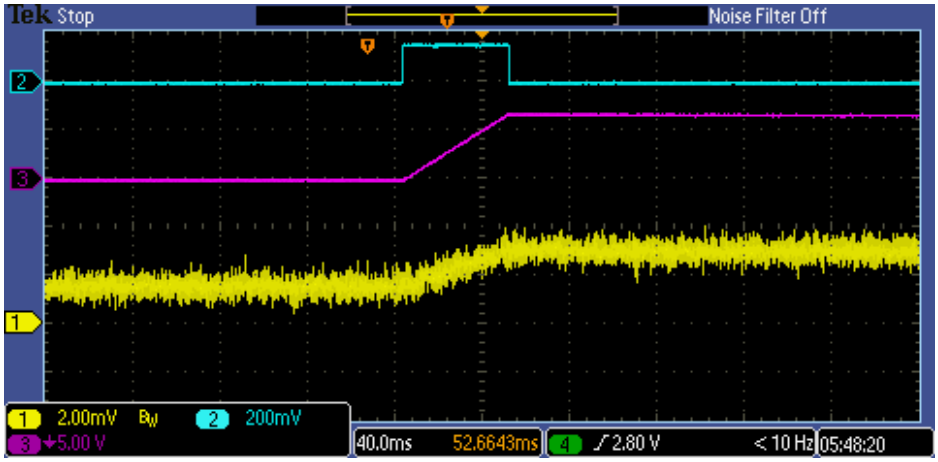

Figure 17. Channel – Channel Perceived Response due to Ground Loop

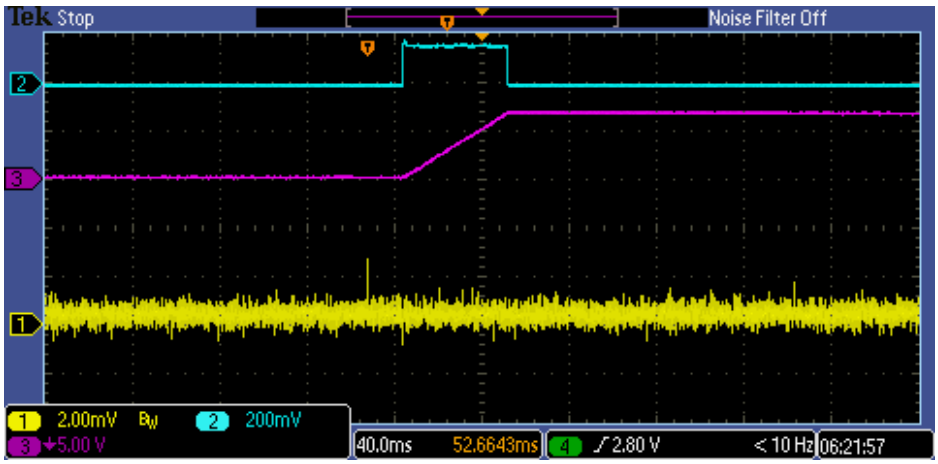

Figure 18. No Channel – Channel Perceived Crosstalk with Differential Probe