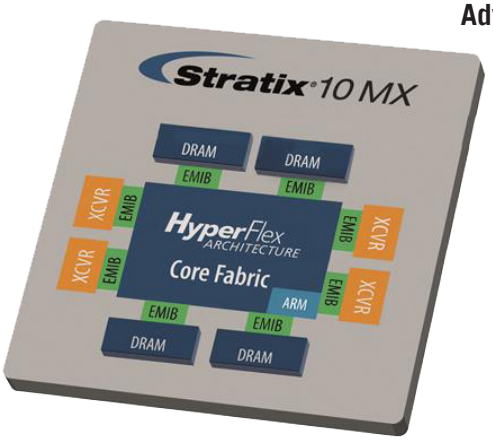
Proc10M

Ultra-High Performance Stratix10MX Module

Advanced Information

Key Features

- Large HBM2 FPGA with ultra-compact module (95mm x 110mm / 3.74" x4.33")
- Flexible usage:
  - Using customized carrier card
  - Using Gidel's carrier card
- Stratix 10MX 2100 HBM2 FPGA:
  - 2,073,000 LEs
  - 7,920 18 x19 MAC
- 5-level memory scheme:
  - Total Throughput > 50TB/s
  - Total capacity > 128GB
- 72 Transceivers with bandwidth > 1,600 Gb/s (TX+RX):
  - 48 x up to 26 Gb/s
  - 16 x up to 16 Gb/s or PCIe Gen3x16
  - 8 x up to 16Gb/s
  - Option for 64 x up to 26 Gb/s
- 356 I/Os supporting:
  - 16 - 3.3V IOs
  - 90 - LVDS (1.6Ghz/line) or 180 GPIO
  - 72 bit DDR4 interface or 156 GPIO
- PLLs with jitter cleaners(100fs)
- 6 dedicated input reference clocks
- 4 output reference clocks
- Supports up to 120W (10A @12V)
- Passive or active cooling
- May be used on half-length PCIe carrier board
- Supported by Gidel ProcWizard (via a PCIe connection)



The Startix10 MX offers 10X more DRAM and eSRAM bandwidth than discrete DDR4 and QDR memories. Gidel's Proc10M module is designed to enable easy use and immediate accessibility to this powerful technology for both computer-based and embedded systems.

The combination of the Proc10M's large FPGA with 10X memory bandwidth and 1,600 Gb/s IO enables unprecedented level of processing, system compactness and cost performance. The powerful Proc10M opens the way to implement diverse innovations and high-end applications, including:

- Compact **Broadcast** and **Image-Processing** solutions enabling to grab data from multiple fast edge sensors and to perform image enhancements, processing, recognition, compression and AI inferences.
- **5G** and **Radar** combining high-speed digital I/O interfaces and edge computing such as FFTs to selectively reduce data and offload it via PCIe x16 or dedicated links.
- **Ultra-fast switch** for wireline traffic management up to 800G and single device solution for Deep Packet Inspection (DPI)
- **AI training** leveraging 128GB density, HBM2s' huge bandwidth and the FPGA's massive logic and DSP blocks.

High-end solutions can be achieved within remarkable short time using the Proc10M module, its carrier boards and Gidel's powerful development suite, thus significantly accelerating the time to market and improving the ROI.

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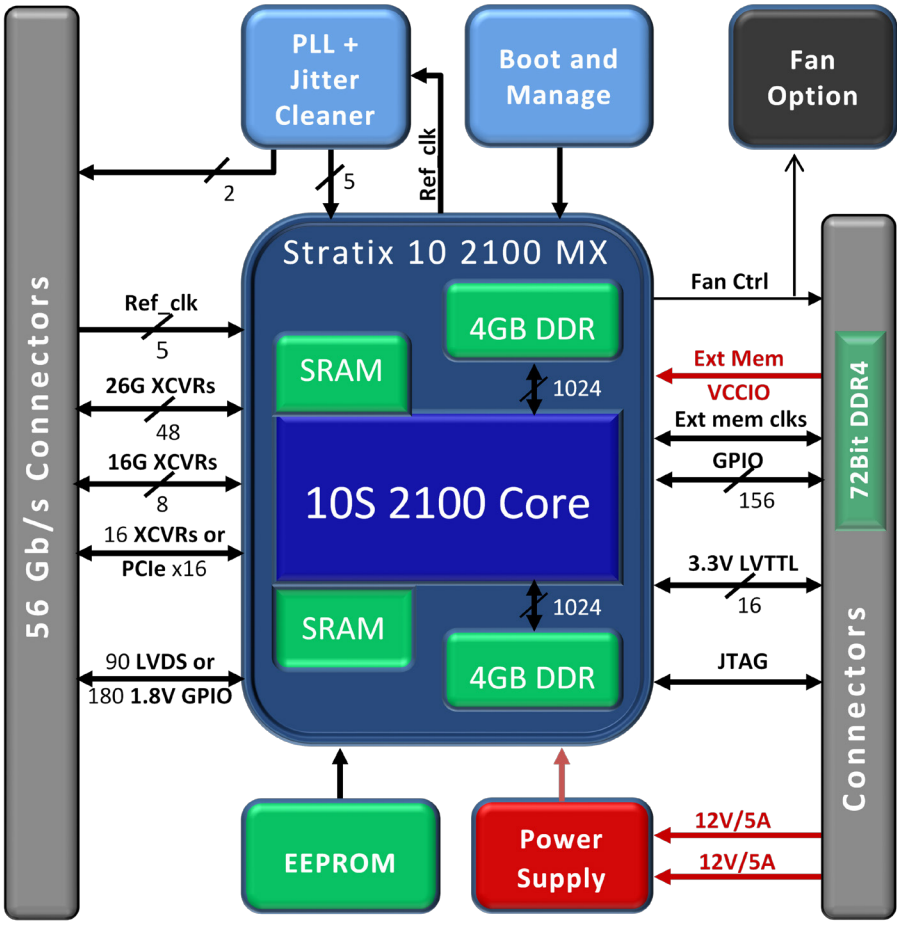
Gidel Developer's Suite

The Gidel Developer's suite comprises tools, IPs and libraries for optimizing performance and reducing FPGA based system development time. Gidel's IPs includes compression, data acquisition and real-time processing, multi-sensor/camera acquisition and synchronization, and a powerful debug IP. Gidel's Developer's suite includes:

- **Proc Dev Kit** for automatic generation of Application Support Package (ASP). By mapping the board resources into the application needs, user may focus on the primary tasks and achieve optimal performance at minimal time. In addition, the kit supports parallel access of multiple applications on a single FPGA thus expediating further the development and improving system reliability.
- **ProcVision Kit** enables different frame grabbing flavors and customization for both software and FPGA design code. Gidel offers a solution for grabbing and synchronizing between100+ cameras. The kit also includes Gidel's CamSim (camera simulator) and CertifEye for debug and verification of FPGA's Image Processing IPs.
- **TotalHistory** debug IP for virtually infinite FPGA signal visibility.
- **Carrier Boards** for the Proc10M module enabling different interface flavors including networking.



Proc10M Block Diagram

Name	Units	Total Capacity	Max Total Throughput
MLAB	17K	11Gb	50 TB/s
M20K	16.8K	134 Gb	41 TB/s
eSRAM	2	94.5Mb	108 GB/s
HBM2 DDR	2	8GB	512 GB/s
DDR4 on carrier board	1	Up to 128GB with ECC	15 GB/s

Memory Performance

International Distributors

Sky Blue Microsystems GmbH
Geisenhausenerstr. 18
81379 Munich, Germany
+49 89 780 2970, info@skyblue.de
www.skyblue.de

In Great Britain:
Zerif Technologies Ltd.
Winnington House, 2 Woodberry Grove
Finchley, London N12 0DR
+44 115 855 7883, info@zerif.co.uk
www.zerif.co.uk