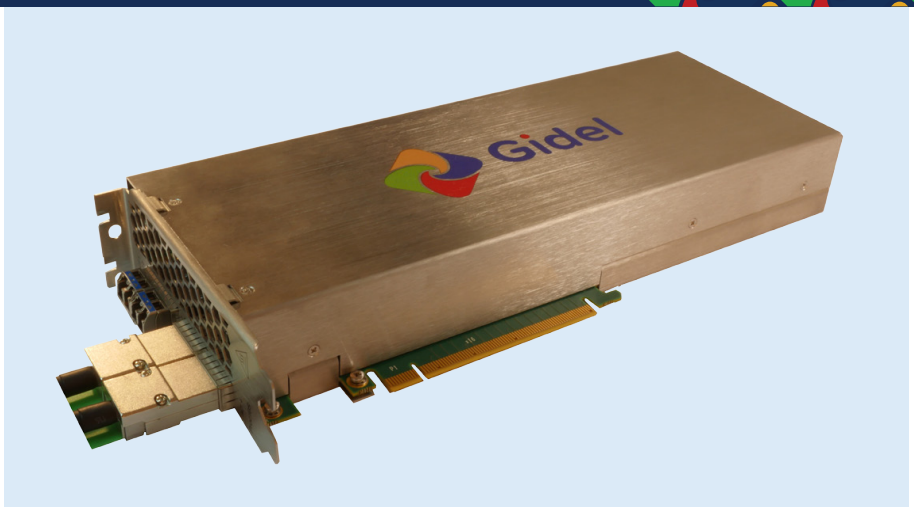
# Proc10S

## High Performance Scalable Compute Accelerators

### Key Features

- Stratix 10 GX/SX FPGA
- Up to 2800K logic elements
- For SX devices, Quad-core 64-bit ARM Cortex-A53 MPCore processor
- PCIe x16 Gen. 3 or stand-alone
- Up to 10× 26 Gb/s + 8x 17.4 Gb/s reconfigurable transceivers (total of 400 Gb/s)
- Form factor: Full-height, double-width, ¾ Length PCI Express card
- Supports up to 12V/300W
- 2x QSFP28, 2x SFP28 and Gidel high-speed connectors
- Multi-level memory structure(260+ GB):
  - Enhanced MLAB (640-bit) SRAM (15 Mb) @ up to 20 Gb/s/block
  - Up to 11,721 M20K (20K-bit) SRAM (229 Mb) @ up to 32 Gb/s/block
  - 4 GB DDR4 SDRAM on-board memory at a maximum sustained throughput of 108 Gb/s
  - 256 GB DDR4 SDRAM (2xRDIMM banks) for maximum sustained throughput of 400 Gb/s
  - Configuration Flash, Serial Flash (SPI) and Serial EEPROM.
- Max. fabric clock freq: 1 GHz
- Flexible clocking system
- Supported by Gidel's OpenCL BSP and HLS (I++) ASP based on Intel's SDK
- Supported by Gidel's Developer's Kit
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications




Gidel's latest high-performance scalable compute acceleration system, the Proc10S, pushes data processing power to new heights with peak single precision performance of up to 10 TFLOPS. The Proc10S features an Intel Stratix 10 FPGA with up 2.8 million logic elements, 260 GB DDR4 memory, and option for SoC Quad-core 64-bit ARM Cortex-A53 MPCore processor . The Proc10S boasts a 16-lane PCIe Gen. 3 host interface and 26 Gb/s and 17.4 Gb/s SERDES I/O transceivers for ultra-fast data injection to the FPGA. Abundant transceiver I/O connectivity enabling a total of 400 Gb/s includes: 2x QSFP28, 2x SFP28 and Gidel proprietary high-speed connectors.

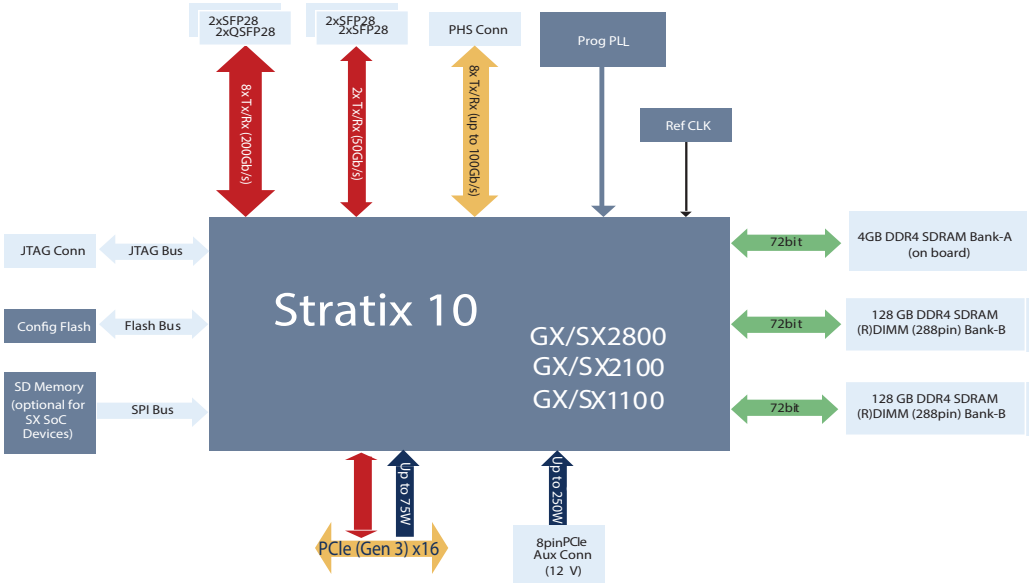
The Proc10S offers designers huge logic resources with incredible flexibility and performance capabilities to meet the most demanding design requirements. The Proc10S can address the design challanges of virtually all end markets including HPC, storage, broadcast, medical, and test and measurement.

The Proc10S is supported by Gidel's unique proprietary tools for developing on FPGA. These tools offer a solution that is unique in the market and can be used together with Intel's design tools to achieve unmatched development efficacy and efficiency. The Gidel development tools suite includes Gidel's Developer's kit as well as OpenCL BSP and HLS (i++) ASP based on Intel's SDK.

# Proc10S - High Performance Scalable Compute Accelerators

| FEATURE | SPECIFICATIONS |
|---|---|
| **FPGA** | • Intel Stratix 10 GX and SX 2800/2100/1100<br>• Up to 2800K Logic Elements<br>• H-TILE supporting up to 26Gb/s SERDES I/O<br>• For SX devices, Quad-core 64 bit ARM Cortex-A53 MPCore processor |
| **Memory** | • Embedded MLAB (640-bit) SRAM blocks<br>• 11,721 M20K (20K-bit) SRAM blocks<br>• Up to 256 GB DDR4 SDRAM (2x (R)DIMMs)<br>• On board 4 GB DDR4 SDRAM |
| **Processing Performance** | • Peak fixed-point performance 23.0 TMACS<br>• Peak floating-point performance 9.2 TFLOPS<br>• M20K blocks at up 32Gb/s per block<br>• MLAB blocks at up to 20Gb/s per block<br>• 4 GB DDR4 SDRAM for total of108 Gb/s<br>• Up to 256 GB DDR4 SDRAM for a total of 400 Gb/s<br>• Up to 11,520 18x19 Variable Precision Multipliers<br>• Up to 10x 26 Gb/s + 8x 17.4 Gb/s reconfigurable transceivers<br>• Quad-core 64 bit ARM Cortex-A53 MPCore @ max processor speed of 1.5 GHz |

| FEATURE | SPECIFICATIONS |
|---|---|
| **Form Factor** | Full-height, double-width, ¾ Length PCI Express |
| **Host Interface** | PCIe x16 Gen.3 |
| **I/O** | • 2x SFP28 + 2x QSFP28<br>• Gidel's High Speed Connector (PHS) |
| **Board Management** | • Flexible clocking system<br>• Temperature monitoring<br>• Internal Voltage monitoring |
| **Development Tools** | • OpenCL BSP based on Intel's SDK<br>• HLS ASP for use with Intel's HLS compiler<br>• Gidel ProDev Kit for HDL design flow:<br>  • Generation of dedicated application driver.<br>  • Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic.<br>  • Generation of environment FPGA code, including all board/IP constrains and user logic wrapper<br>• Intel Tools: Quartus Prime Pro including QSys and DSP builder |




## Proc10S System Block Diagram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