Proc10S

High Performance Scalable Compute Accelerators

Key Features

- Stratix 10 SX FPGA
- Up to 2800K logic elements
- Quad-core 64-bit ARM Cortex-A53 MPCore processor
- PCIe x16 Gen. 3 or stand-alone
- Up to 16x 28.3 Gb/s reconfigurable transceivers (total of 452 Gb/s)
- Form factor: Full-height, double-width, ¾ Length PCI Express card
- Supports up to 245 W (including I/Os): 65W via PCIe, 180W via external source
- I/O Options: 4x QSFP28, 2x SFP28, RGMII and Gidel high-speed connector
- Multi-level memory structure(260+ GB):
  - Enhanced MLAB (640-bit) SRAM
  - Up to 11,721 M20K (20K-bit) SRAM (229 Mb) @ up to 58 TB/s sust. access
  - 4 GB DDR4 SDRAM on-board memory at a maximum sustained throughput of 13.5 GB/s
  - Up to 256 GB DDR4 SDRAM (2x(U/R) DIMM banks) for maximum sustained throughput of 48 GB/s
  - Configuration Flash
  - Serial Flash (SPI)
- Max. fabric clock freq: 1 GHz
- Flexible clocking system with dual ultra-low jitter attenuator @ 100 fsec
- Passive or active cooling
- Supported by Gidel's Developer's Kit
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications
- Supports Intel development tools

Gidel's latest high-performance scalable compute acceleration system, the Proc10S, pushes data processing power to new heights with peak single precision performance of up to 10 TFLOPS. The Proc10S features an Intel Stratix 10 FPGA with up to 2.8 million logic elements, 260 GB DDR4 memory, and an option for SoC Quad-core 64-bit ARM Cortex-A53 MPCore processor . The Proc10S boasts a 16-lane PCIe Gen. 3 host interface and 28.3 Gb/s and 14.1 Gb/s SERDES I/O transceivers for ultra-fast throughput of up to 452 Gb/s. Abundant I/O connectivity options include: 4x QSFP28 or a combination of 2xQSFP28, 2x SFP28 and RGMII/ Gidel proprietary high-speed connector.

The Proc10S offers designers huge logic resources with incredible flexibility and performance capabilities to meet the most demanding design requirements. The Proc10S can address the design challanges of virtually all end markets including HPC, storage, broadcast, medical, and test & measurement.

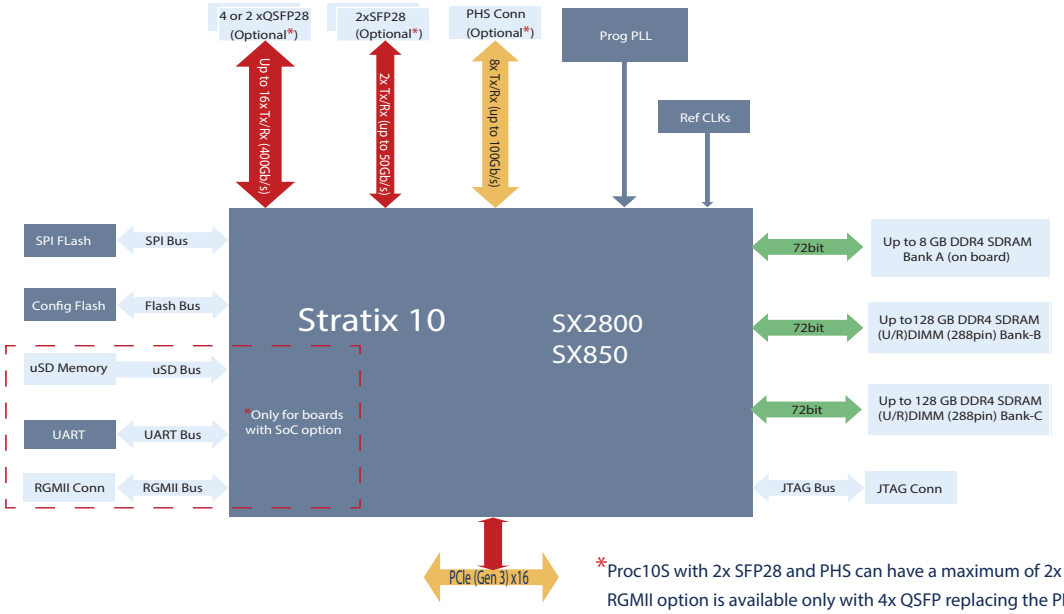
The Proc10S is supported by Gidel's unique proprietary tools for developing on FPGA. These tools offer a solution that is unique in the market and can be used together with Intel's design tools to achieve unmatched development efficacy and efficiency. The Gidel development tools suite includes the Gidel ProcWizard for automatic generation and integration of HDL and software code as well as Gidel proprietary IPs, including data-compression-decompression IPs, efficient data management IPs and more.

Proc10S - High Performance Scalable Compute Accelerators

FEATURE	SPECIFICATIONS
FPGA	• Intel Stratix 10 SX 2800/850 • Up to 2800K Logic Elements • H-TILE supporting up to 28.3 Gb/s SERDES I/O • For SX devices, Quad-core 64 bit ARM Cortex-A53 MPCore processor
Memory	• Embedded MLAB (640-bit) SRAM blocks • 11,721 M20K (20K-bit) SRAM blocks • Up to 256 GB DDR4 SDRAM (2x (U/R)DIMMs) • On board - up to 4 GB DDR4 SDRAM
Performance	• Peak fixed-point performance 23.0 TMACS • Peak floating-point performance 9.2 TFLOPS • M20K blocks at up to 58 TB/s sustain access • On board DDR4 SDRAM at up to 13.5 GB/s • (U/R)DIMMs DDR4 SDRAM at up to 48 GB/s • Up to 11,520 18x19 Variable Precision Multipliers • Up to 16x 28.3 Gb/s reconfigurable transceivers • Quad-core 64 bit ARM Cortex-A53 MPCore @ max processor speed of 1.5 GHz • Dual jitter attenuators with accuracy of 100 fs

FEATURE	SPECIFICATIONS
Form Factor	Full-height, double-width, ¾ Length PCI Express
Host Interface	PCIe x16 Gen.3
I/O*	• 4x QSFP28 or 2x QSFP28, 2x SFP28 and Gidel High Speed interface (PHS) • RGMII
Board Management	• Flexible clocking system • Temperature monitoring • Internal Voltage monitoring

Development Tools	• Gidel ProDev Kit for HDL design flow:
	  • Generation of dedicated application driver.
	  • Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic.
	  • Generation of environment FPGA code, including all board/IP constrains and user logic wrapper
	  • Automatic generation and integration of Gidel IPs, including compresssion/decompression IPs, memory controller & data processing IPs, and more
	• Intel Tools: Quartus Pro, QSys and DSP builder



*Proc10S with 2x SFP28 and PHS can have a maximum of 2x QSFP.
RGMII option is available only with 4x QSFP replacing the PHS interface.

Proc10S System Block Diagram

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