CoaXPress Multi-Link Multi-Stream FPGA IP Core

Overview

The CoaXPress IP Core from KAYA Instruments provides a Multi-link high performance solution for rate demanding video applications. Both Host and Device modes of operation are supported. The IP core offers support for newest and industry leading FPGAs from Xilinx, Intel and Microsemi. The device IP core incorporates a friendly streaming interface with highly configurable pixel packer for glue-less connection to imaging sensor or user logic.

Features

- Compliant with CoaXPress standard rev 2.0 / 1.1 / 1.0
- CXP-12 support of up to 12.5 Gbps high speed link and up to 41.6 Mbps low speed link
- Multiple link rates support
- Supports both Host and Device modes
- Multiple CoaXPress links suited for applications demanding high throughput.
- Multiple video stream support
- Build in FPGA SerDes, no need for additional design effort
- AXI4L/Avalon MM support for control channel
- Highly configurable pixel packer
- Host IP Core supports multiple device connection on different data rates
- Embedded CRC-32 generate/check for streaming data packets
- Avalon and AXI4 Stream Interface Profile in Host IP Core
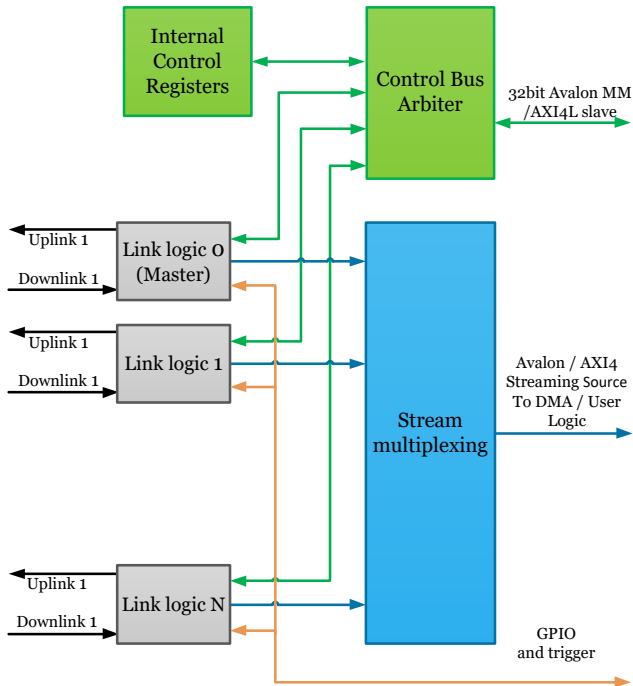- Dedicated ports for GPIO and trigger
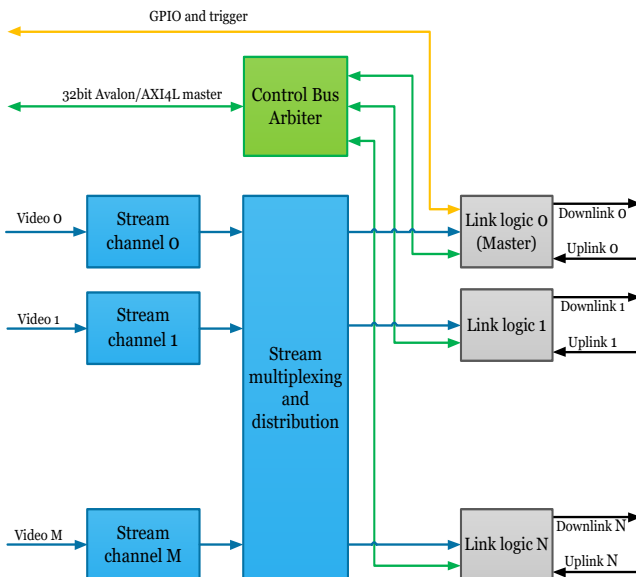
About CoaXPress

CoaXPress is a new digital transmission standard that allows high speed data from a device, such as a camera, to be transferred to a host, such as a frame grabber. Each CoaXPress link supports up to 12.5 Gbps data rates, along with device power up to 13W and device control at 41 Mbps – all on a single coax cable. For very fast devices, the links can be aggregated to provide multiples of the single coax bandwidth. Long cable lengths are supported – up to 30 meters at 12.5 Gbps and over 100 meters at 3.125 Gbps.

Block Diagram

Host CoaXPress FPGA IP Core:

Device CoaXPress FPGA IP Core:

Core Details

- Single or multi-use license
- Free license for KAYA Instruments CXP Mezzanine card users
- Soft IP core: RTL-encrypted source code, synthesis scripts, etc.
- Comprehensive documentation package
- Support for Intel®, Xilinx® and Microsemi® FPGAs
- Language: Verilog HDL
- Simulation environment: ModelSim

Applications

- ✓ High speed cameras
- ✓ High definition cameras
- ✓ Panoramic cameras
- ✓ Upgrade for legacy coax based systems
- ✓ Defense remote systems
- ✓ Slip Ring systems
- ✓ Automotive surround view system
- ✓ Surveillance
- ✓ Robotic Vision

Deliverables

- CoaXPress FPGA IP Core
- Comprehensive usage examples
- Reference design
- Bootstrap register file with optional I2C/SPI IP Core