FPGA Mezzanine Card for CoaXPress™

Data Book
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International Distributors

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Revision History

Version	Date	Notes
0.1	10.3.13	Initial Release
1.0	31.3.14	Minor updates for second edition (Rev 2)
1.1	16.9.14	Minor updates for third edition (Rev 3)
1.2	29.3.15	Correction to the FMC connector pin assignments table
1.3	31.7.16	Added PoCXP circuit. Support for 1.8V I/O voltage (Rev 4)
1.4	10.7.17	I/O voltages updated
1.5	10.12.17	Minor updates for the fifth edition (Rev 5)
1.6	28.4.18	Minor updates for the fifth edition (Rev 5)

2.1 Safety Precautions

With your ***FPGA Mezzanine Card for CoaXPress™ (KY-FMCCXP)*** board in hand, please take a minute to read carefully the precautions listed below in order to prevent unnecessary injuries to you or other personnel or cause damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to act upon it to prevent misuse of product.**

Caution

In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Do not use or place the product in the following locations. ● Humid and dusty locations ● Airless locations such as closet or bookshelf ● Locations which receive oily smoke or steam ● Locations close to heating equipment ● Closed inside of a car where the temperature becomes high ● Static electricity replete locations ● Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
Do not place heavy things on the product. Otherwise, the product may be damaged.

2.2 Disclaimer

This product should be used for CoaXPress video acquisition and generation. It also can be used for digital input/output (GPIO) purposes. KAYA Instruments assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, KAYA Instruments assumes no responsibility for any damages caused by the following:

- Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts caused by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- Secondary impact arising from use of this product or its unusable state (business interruption or others).
- Use of this product against the instructions given in this manual or malfunctions due to connection to other devices.

KAYA Instruments assumes no responsibility or liability for:

- Erasure or corruption of data arising from use of this product.
- Any consequences or other abnormalities arising from use of this product, or damage of this product not due to our responsibility or failure due to modification.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

3 Key Features

3.1 Overview

The ***KY-FMCCXP*** is the industry's first FPGA Mezzanine Card (VITA 57.1) providing a high performance CoaXPress compliant connection. The ***KY-FMCCXP*** is capable of capturing video from up to 5 CoaXPress mode cameras and is ideally suited to industrial, defense and aerospace applications. This mezzanine card might be also used as camera simulator, emulating up to 5 transmitting channels. Customer specific data pre-processing or custom protocols are easily accommodated via FPGA carrier card. The ***KY-FMCCXP*** also provides GPIO for input/output signals (optionally isolated), such as triggers, shaft encoders, exposure control and general I/O.

The ***KY-FMCCXP*** uses a high-pin count connector (HPC) as an interface to the host board, general purpose I/O and can be used in a ruggedized conduction cooled factor for harsher environments. Up to 5 host/device links can be provided using front panel DIN 1.0/2.3 connectors. Each link supports standard CoaXPress bitrates up to 6.25 Gbps. Each host link is capable of providing up to 13W of power to compatible devices via Power over CoaXPress (PoCXP). The ***KY-FMCCXP*** can support up to 5 individual links, or combinations of aggregated CoaXPress links (e.g. one camera requiring one link, and two additional cameras each using two links).

3.2 Features

- Interfaces:
  - Up to 5 CoaXPress links
  - Each link can be host or device (configuration specific)
  - 6 LVTTL inputs (optionally opto-isolated)
  - 6 LVTTL outputs (optionally opto-isolated)
  - External power supply for extended use of power over CoaXPress (optional)
- VITA 57.1 compliant
- Conduction or air cooled
- 5 x DIN 1.0/2.3 connectors available from the front panel
- MIL-I-46058c conformal coating (optional)
- HPC – High Pin count connector
- Power over CoaXPress support with short circuit protection
- Support standard CoaXPress data rates up to 6.25Gpbs
- -40°C to 85°C operating environment temperature (industrial grade)

3.3 Product Applications

- ✓ High speed cameras
- ✓ High definition cameras
- ✓ Panoramic cameras
- ✓ Existing coax systems upgrade
- ✓ Defense remote systems
- ✓ Slip Ring systems
- ✓ Automotive surround view system
- ✓ Surveillance
- ✓ Robotic Vision

3.4 Related documents and accessories

Documents:

- EQCO62R20.3 Datasheet from Microchip (EqcoLogic)
- EQCO62T20.3 Datasheet from Microchip (EqcoLogic)
- American National Standard for FPGA Mezzanine Card (FMC) Standard (ANSI/VITA 57.1-2008)
- Two-wire Serial EEPROM 1K (AT24C01B)

Optional accessories:

- Board Standoffs set
- Transmission cable set
  - DIN-BNC : 1
  - DIN-DIN : 1

4.1 Block Diagram

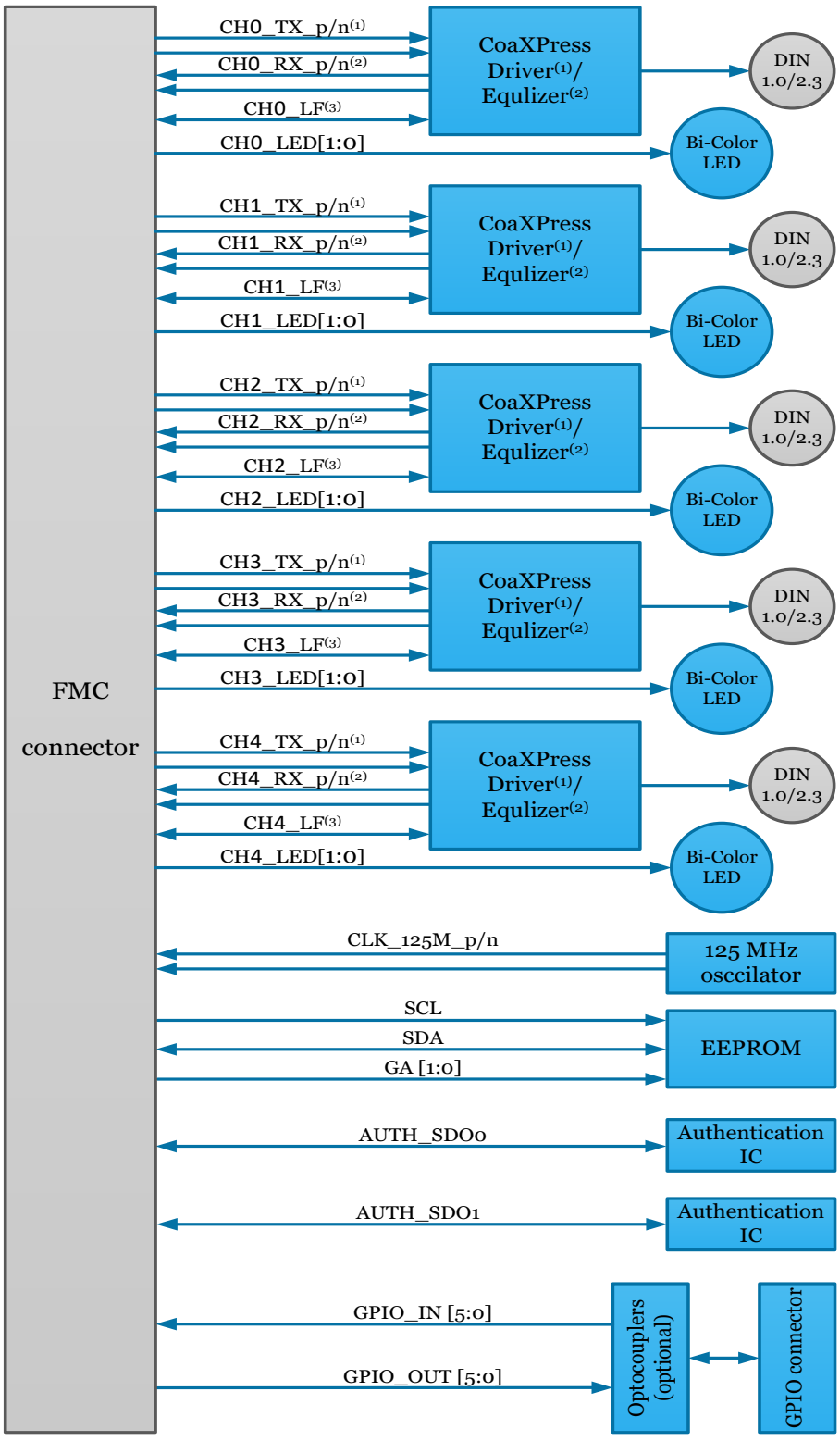

Figure 1 : KY-FMCCXP block diagram

4.2 External View of the Board

Figure 2 shows the ***KY-FMCCXP*** board specification.

External Dimensions: Width: 63mm x Height: 84mm

Board Thickness: 1.6mm

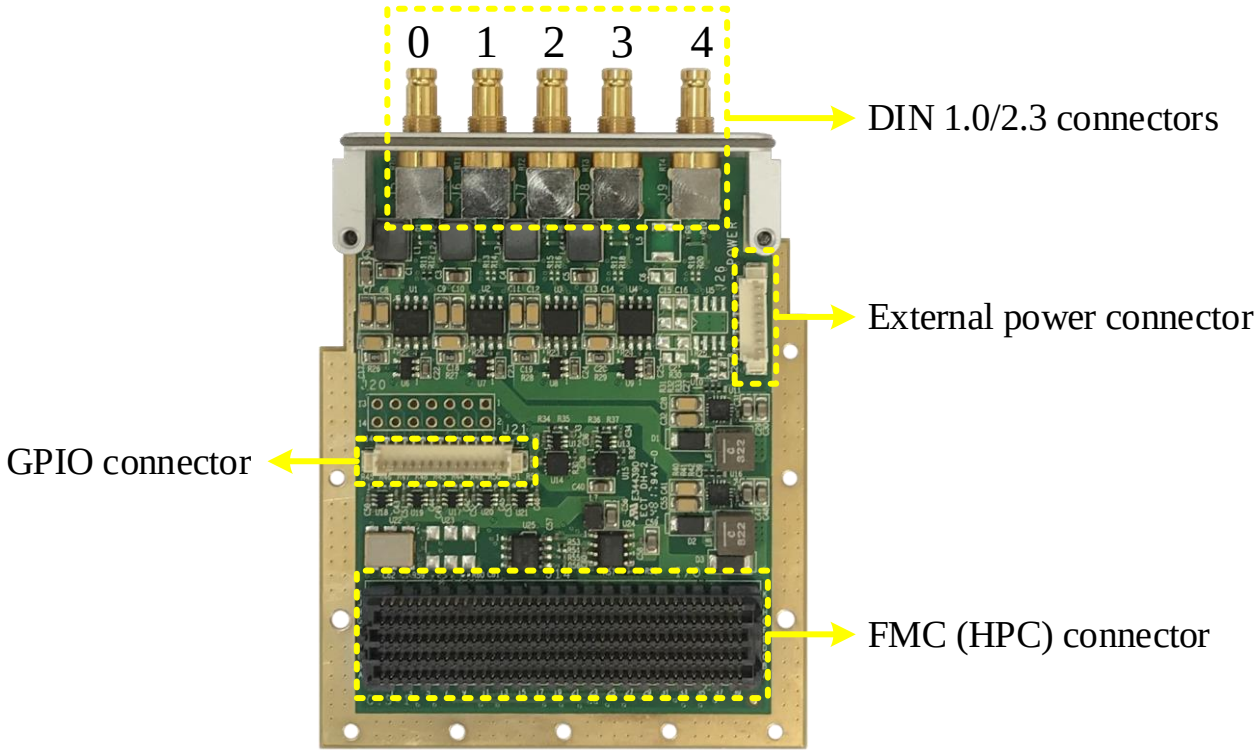

Figure 2 : KY-FMCCXP external view

4.3 Power supply to the board

Figure 3 shows the power supply circuit of the ***KY-FMCCXP*** board. The board receives +3.3V from the FMC connector and dispenses it to the GPIO and Drivers. A +12V from the FMC connector converted into +1.2V which proceed to Driver and Equalizers. Channels 0 and 1 receive 24V from shared power supply. As where Channels 2, 3 and 4 receive 24V from other shared power supply.

The 24V power supplies can be powered from the FMC connector or from external connector for power demanding applications.

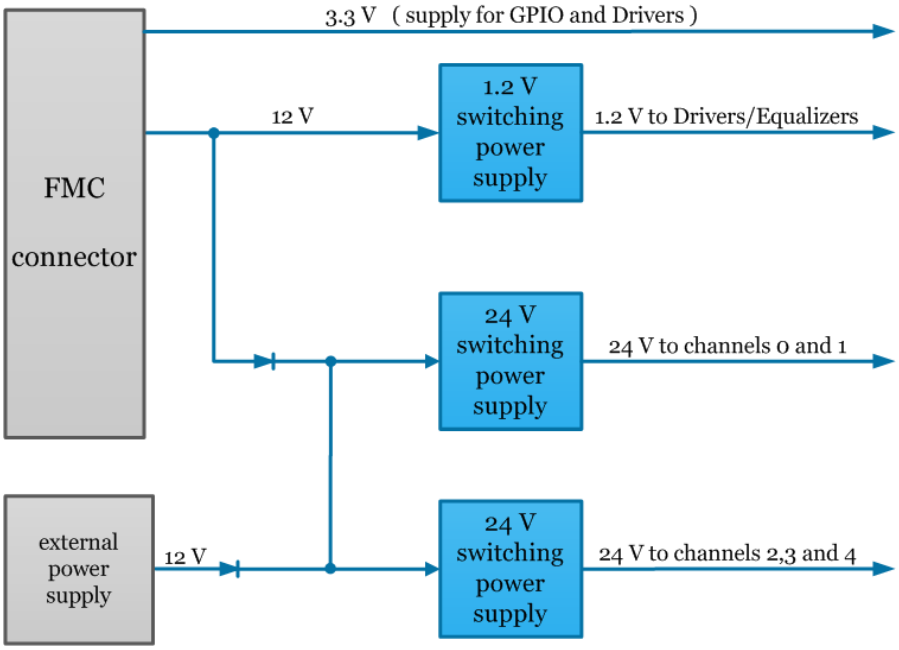

Figure 3 : KY-FMCCXP power supply dispense

Each Host CoaXPress link has PoCXP compatibility and is able to provide up to 13.5W of power per each link to the camera. Each link implements a PoCXP circuit as following:

- Short circuit protection that disables the PoCXP output if the current drawn from the link is larger than 0.9A.
- Current source for link detection
- Voltage measurement
- Current measurement

It is up to the customer to implement to PoCXP detection logic according to the CoaXPress standard. The simplified algorithm for specific channel should be as following:

(1) Set ON pin to 1 (Disable PoCXP)
(2) Periodically measure VOLTAGE_SENSE with the ADC
(3) If the voltage is within a threshold set ON pin to 0 (Enable PoCXP)
(4) Periodically measure CURRENT_SENSE with ADC
(5) If current falls below a threshold set ON to 1 (Disable PoCXP)

NOTE: The PoCXP can be forced to "On" or "Off" by simply setting the ON pin to 0 or 1 without any detection logic. If PoCXP is forced "On", please pay attention not to hot plug the camera as it may result in permanent damage to the camera.

The PoCXP related logic diagram can be seen in Figure **4**, while for measuring the current and voltage of the channels ADS7828E ADC from TI are used. The ADS7828E are connected to the FPGA with an FMC dedicated I2C interface via C30 and C31 FMC connector pins. The ADC have the following channel mapping:

ADC	I2C address (8bit)	Channel	Function
0	0x90	0	CH0_VOLTAGE_SENSE
0	0x90	1	CH0_CURRENT_SENSE
0	0x90	2	CH1_VOLTAGE_SENSE
0	0x90	3	CH1_CURRENT_SENSE
0	0x90	4	CH2_VOLTAGE_SENSE
0	0x90	5	CH2_CURRENT_SENSE
0	0x90	6	CH3_VOLTAGE_SENSE
0	0x90	7	CH3_CURRENT_SENSE
1	0x91	0	CH4_VOLTAGE_SENSE
1	0x91	1	CH4_CURRENT_SENSE
1	0x91	2	Not used
1	0x91	3	Not used
1	0x91	4	Not used
1	0x91	5	Not used
1	0x91	6	Not used
1	0x91	7	Not used

Table 1 : PoCXP ADC channel mapping

5.1 FMC (HPC) pin assignments

Carrier board FMC connector pin assignments. The direction is according to carrier (FPGA) side. The connector PN is ASP-134488-01 from Samtec. The standard FMC pin assignment of the connector is described in Table 2.

#	FMC Spec	I/O	Signal Name	Description
A1	GND	-	-	Signal Ground
A2	DP1_M2C_P	I	CH1_RXp	CoaXPress channel 1 fast speed link Receive (Positive) (2)
A3	DP1_M2C_N	I	CH1_RXn	CoaXPress channel 1 fast speed link Receive (Negative) (2)
A4	GND	-	-	Signal Ground
A5	GND	-	-	Signal Ground
A6	DP2_M2C_P	I	CH2_RXp	CoaXPress channel 2 fast speed link Receive (Positive) (2)
A7	DP2_M2C_N	I	CH2_RXn	CoaXPress channel 2 fast speed link Receive (Negative) (2)
A8	GND	-	-	Signal Ground
A9	GND	-	-	Signal Ground
A10	DP3_M2C_P	I	CH3_RXp	CoaXPress channel 3 fast speed link Receive (Positive) (2)
A11	DP3_M2C_N	I	CH3_RXn	CoaXPress channel 3 fast speed link Receive (Negative) (2)
A12	GND	-	-	Signal Ground
A13	GND	-	-	Signal Ground
A14	DP4_M2C_P	I	CH4_RXp	CoaXPress channel 4 fast speed link Receive (Positive) (2)
A15	DP4_M2C_N	I	CH4_RXn	CoaXPress channel 4 fast speed link Receive (Negative) (2)
A16	GND	-	-	Signal Ground
A17	GND	-	-	Signal Ground
A18	DP5_M2C_P	-	N/C	Not Connected
A19	DP5_M2C_N	-	N/C	Not Connected
A20	GND	-	-	Signal Ground
A21	GND	-	-	Signal Ground
A22	DP1_C2M_P	O	CH1_TXp	CoaXPress channel 1 fast speed link Transmit (Positive) (1)
A23	DP1_C2M_N	O	CH1_TXn	CoaXPress channel 1 fast speed link Transmit (Negative) (1)
A24	GND	-	-	Signal Ground
A25	GND	-	-	Signal Ground
A26	DP2_C2M_P	O	CH2_TXp	CoaXPress channel 2 fast speed link Transmit (Positive) (1)
A27	DP2_C2M_N	O	CH2_TXn	CoaXPress channel 2 fast speed link Transmit (Negative) (1)
A28	GND			
A29	GND	-	-	Signal Ground
A30	DP3_C2M_P	O	CH3_TXp	CoaXPress channel 3 fast speed link Transmit (Positive) (1)
A31	DP3_C2M_N	O	CH3_TXn	CoaXPress channel 3 fast speed link Transmit (Negative) (1)
A32	GND	-	-	Signal Ground
A33	GND	-	-	Signal Ground
A34	DP4_C2M_P	O	CH4_TXp	CoaXPress channel 4 fast speed link Transmit (Positive) (1)
A35	DP4_C2M_N	O	CH4_TXn	CoaXPress channel 4 fast speed link Transmit (Negative) (1)
A36	GND	-	-	Signal Ground
A37	GND	-	-	Signal Ground
A38	DP5_C2M_P	-	N/C	Not Connected
A39	DP5_C2M_N	-	N/C	Not Connected
A40	GND	-	-	Signal Ground
B1	RES1	-	N/C	Not Connected
B2	GND	-	-	Signal Ground
B3	GND	-	-	Signal Ground
B4	DP9_M2C_P	-	N/C	Not Connected

B5	DP9_M2C_N	-	N/C	Not Connected
B6	GND	-	-	Signal Ground
B7	GND	-	-	Signal Ground
B8	DP8_M2C_P	-	N/C	Not Connected
B9	DP8_M2C_N	-	N/C	Not Connected
B10	GND	-	-	Signal Ground
B11	GND	-	-	Signal Ground
B12	DP7_M2C_P	-	N/C	Not Connected
B13	DP7_M2C_N	-	N/C	Not Connected
B14	GND	-	-	Signal Ground
B15	GND	-	-	Signal Ground
B16	DP6_M2C_P	-	N/C	Not Connected
B17	DP6_M2C_N	-	N/C	Not Connected
B18	GND	-	-	Signal Ground
B19	GND	-	-	Signal Ground
B20	GBTCLK1_M2C_P	-	GND	Pulled to GND
B21	GBTCLK1_M2C_N	-	VADJ	Adjustable voltage for I/O signals to FPGA
B22	GND	-	-	Signal Ground
B23	GND	-	-	Signal Ground
B24	DP9_C2M_P	-	N/C	Not Connected
B25	DP9_C2M_N	-	N/C	Not Connected
B26	GND	-	-	Signal Ground
B27	GND	-	-	Signal Ground
B28	DP8_C2M_P	-	N/C	Not Connected
B29	DP8_C2M_N	-	N/C	Not Connected
B30	GND	-	-	Signal Ground
B31	GND	-	-	Signal Ground
B32	DP7_C2M_P	-	N/C	Not Connected
B33	DP7_C2M_N	-	N/C	Not Connected
B34	GND	-	-	Signal Ground
B35	GND	-	-	Signal Ground
B36	DP6_C2M_P	-	N/C	Not Connected
B37	DP6_C2M_N	-	N/C	Not Connected
B38	GND	-	-	Signal Ground
B39	GND	-	-	Signal Ground
B40	RES0	-	N/C	Not Connected
C1	GND	-	-	Signal Ground
C2	DP0_C2M_P	O	CH0_TXp	CoaXPress channel 0 fast speed link Transmit (Positive) (1)
C3	DP0_C2M_N	O	CH0_TXn	CoaXPress channel 0 fast speed link Transmit (Negative) (1)
C4	GND	-	-	Signal Ground
C5	GND	-	-	Signal Ground
C6	DP0_M2C_P	I	CH0_RXp	CoaXPress channel 0 fast speed link Receive (Positive) (2)
C7	DP0_M2C_N	I	CH0_RXn	CoaXPress channel 0 fast speed link Receive (Negative) (2)
C8	GND	-	-	Signal Ground
C9	GND	-	-	Signal Ground
C10	LA06_P	O	GPIO_OUT3	GPIO output 3
C11	LA06_N	O	GPIO_OUT2	GPIO output 2
C12	GND	-	-	Signal Ground
C13	GND	-	-	Signal Ground
C14	LA10_P	I	GPIO_IN5	GPIO input 5
C15	LA10_N	I	GPIO_IN4	GPIO input 4
C16	GND	-	-	Signal Ground
C17	GND	-	-	Signal Ground
C18	LA14_P	O	CH3_LED0	Link 3 Green indicator LED (Active low)
C19	LA14_N	O	CH3_LED1	Link 3 Red indicator LED (Active low)
C20	GND	-	-	Signal Ground
C21	GND	-	-	Signal Ground
C22	LA18_P_CC	I	CH0_FLAGB	Channel 0 PoCXP indicator (Active high)

C23	LA18_N_CC	I	CH4_PWRG	Channel 4 PoCXP power good indicator (Active high)
C24	GND	-	-	Signal Ground
C25	GND	-	-	Signal Ground
C26	LA27_P	-	N/C	Not Connected
C27	LA27_N	-	N/C	Not Connected
C28	GND	-	-	Signal Ground
C29	GND	-	-	Signal Ground
C30	SCL	O	SCL	I2C clock Connected to Identification EEPROM and PoCXP ADCs
C31	SDA	I/O	SDA	I2C data Connected to Identification EEPROM and PoCXP ADCs
C32	GND	-	-	Signal Ground
C33	GND	-	-	Signal Ground
C34	GA0	O	GA0	Connected to Identification EEPROM
C35	12P0V	-	12V	12V power supply
C36	GND	-	-	Signal Ground
C37	12P0V	-	12V	12V power supply
C38	GND	-	-	Signal Ground
C39	3P3V	-	3.3V	3.3V Power supply
C40	GND	-	-	Signal Ground
D1	PG_C2M	-	N/C	Not Connected
D2	GND	-	-	Signal Ground
D3	GND	-	-	Signal Ground
D4	GBTCLK0_M2C_P	I	CLK_125M_P	125MHz Reference clock (Positive)
D5	GBTCLK0_M2C_N	I	CLK_125M_N	125MHz Reference clock (Negative)
D6	GND	-	-	Signal Ground
D7	GND	-	-	Signal Ground
D8	LA01_P_CC	I/O	LF2	CoaXPress channel 2 low speed link $TX^{(2)}/RX^{(1)}$
D9	LA01_N_CC	I/O	LF1	CoaXPress channel 1 low speed link $TX^{(2)}/RX^{(1)}$
D10	GND	-	-	Signal Ground
D11	LA05_P	O	GPIO_OUT1	GPIO output 1
D12	LA05_N	O	GPIO_OUT0	GPIO output 0
D13	GND	-	-	Signal Ground
D14	LA09_P	I	GPIO_IN3	GPIO input 3
D15	LA09_N	I	GPIO_IN2	GPIO input 2
D16	GND	-	-	Signal Ground
D17	LA13_P	O	CH2_LED0	Link 2 Green indicator LED (Active low)
D18	LA13_N	O	CH2_LED1	Link 2 Red indicator LED (Active low)
D19	GND	-	-	Signal Ground
D20	LA17_P_CC	I	CH3_PWRG	Channel 3 PoCXP power good indicator (Active high)
D21	LA17_N_CC	I	CH2_PWRG	Channel 2 PoCXP power good indicator (Active high)
D22	GND	-	-	Signal Ground
D23	LA23_P	-	N/C	Not Connected
D24	LA23_N	O	CH4_ON	Channel 4 PoCXP enable (Active low)
D25	GND	-	-	Signal Ground
D26	LA26_P	-	N/C	Not Connected
D27	LA26_N	-	N/C	Not Connected
D28	GND	-	-	Signal Ground
D29	TCK	-	N/C	Not Connected
D30	TDI	-	TD	JTAG Loopback
D31	TDO	-	TD	JTAG Loopback
D32	3P3VAUX	-	3.3V_AUX	Auxiliary 3.3V
D33	TMS	-	N/C	Not Connected
D34	TRST_L	-	N/C	Not Connected
D35	GA1	O	GA1	Connected to Identification EEPROM
D36	3P3V	-	3.3V	3.3V Power supply
D37	GND	-	-	Signal Ground
D38	3P3V	-	3.3V	3.3V Power supply
D39	GND	-	-	Signal Ground
D40	3P3V	-	3.3V	3.3V Power supply

E1	GND	-	-	Signal Ground
E2	HA01_P_CC	-	N/C	Not Connected
E3	HA01_N_CC	-	N/C	Not Connected
E4	GND	-	-	Signal Ground
E5	GND	-	-	Signal Ground
E6	HA05_P	-	N/C	Not Connected
E7	HA05_N	-	N/C	Not Connected
E8	GND	-	-	Signal Ground
E9	HA09_P	-	N/C	Not Connected
E10	HA09_N	-	N/C	Not Connected
E11	GND	-	-	Signal Ground
E12	HA13_P	-	N/C	Not Connected
E13	HA13_N	-	N/C	Not Connected
E14	GND	-	-	Signal Ground
E15	HA16_P	-	N/C	Not Connected
E16	HA16_N	-	N/C	Not Connected
E17	GND	-	-	Signal Ground
E18	HA20_P	-	N/C	Not Connected
E19	HA20_N	-	N/C	Not Connected
E20	GND	-	-	Signal Ground
E21	HB03_P	-	N/C	Not Connected
E22	HB03_N	-	N/C	Not Connected
E23	GND	-	-	Signal Ground
E24	HB05_P	-	N/C	Not Connected
E25	HB05_N	-	N/C	Not Connected
E26	GND	-	-	Signal Ground
E27	HB09_P	-	N/C	Not Connected
E28	HB09_N	-	N/C	Not Connected
E29	GND	-	-	Signal Ground
E30	HB13_P	-	N/C	Not Connected
E31	HB13_N	-	N/C	Not Connected
E32	GND	-	-	Signal Ground
E33	HB19_P	-	N/C	Not Connected
E34	HB19_N	-	N/C	Not Connected
E35	GND	-	-	Signal Ground
E36	HB21_P	-	N/C	Not Connected
E37	HB21_N	-	N/C	Not Connected
E38	GND	-	-	Signal Ground
E39	VADJ	-	VADJ	Adjustable voltage for I/O signals to FPGA
E40	GND	-	-	Signal Ground
F1	PG_M2C	I	3.3V	Pulled to 3.3V
F2	GND	-	-	Signal Ground
F3	GND	-	-	Signal Ground
F4	HA00_P_CC	-	N/C	Not Connected
F5	HA00_N_CC	-	N/C	Not Connected
F6	GND	-	-	Signal Ground
F7	HA04_P	-	N/C	Not Connected
F8	HA04_N	-	N/C	Not Connected
F9	GND	-	-	Signal Ground
F10	HA08_P	-	N/C	Not Connected
F11	HA08_N	-	N/C	Not Connected
F12	GND	-	-	Signal Ground
F13	HA12_P	-	N/C	Not Connected
F14	HA12_N	-	N/C	Not Connected
F15	GND	-	-	Signal Ground
F16	HA15_P	-	N/C	Not Connected
F17	HA15_N	-	N/C	Not Connected
F18	GND	-	-	Signal Ground

F19	HA19_P	-	N/C	Not Connected
F20	HA19_N	-	N/C	Not Connected
F21	GND	-	-	Signal Ground
F22	HB02_P	-	N/C	Not Connected
F23	HB02_N	-	N/C	Not Connected
F24	GND	-	-	Signal Ground
F25	HB04_P	-	N/C	Not Connected
F26	HB04_N	-	N/C	Not Connected
F27	GND	-	-	Signal Ground
F28	HB08_P	-	N/C	Not Connected
F29	HB08_N	-	N/C	Not Connected
F30	GND	-	-	Signal Ground
F31	HB12_P	-	N/C	Not Connected
F32	HB12_N	-	N/C	Not Connected
F33	GND	-	-	Signal Ground
F34	HB16_P	-	N/C	Not Connected
F35	HB16_N	-	N/C	Not Connected
F36	GND	-	-	Signal Ground
F37	HB20_P	-	N/C	Not Connected
F38	HB20_N	-	N/C	Not Connected
F39	GND	-	-	Signal Ground
F40	VADJ	-	VADJ	Adjustable voltage for I/O signals to FPGA
G1	GND	-	-	Signal Ground
G2	CLK0_C2M_P	-	N/C	Not Connected
G3	CLK0_C2M_N	-	N/C	Not Connected
G4	GND	-	-	Signal Ground
G5	GND	-	-	Signal Ground
G6	LA00_P_CC	I/O	LF0	CoaXPress channel 0 low speed link TX(2)/RX(1)
G7	LA00_N_CC	I/O	AUTH_SDO0	Authentication connection 0 to IP Core
G8	GND	-	-	Signal Ground
G9	LA03_P	O	AUTH_DIR_SDO 0	Direction selector for SDO0. High - output
G10	LA03_N	I/O	AUTH_SDO1	Authentication connection 1 to IP Core
G11	GND	-	-	Signal Ground
G12	LA08_P	I	GPIO_IN1	GPIO input 1
G13	LA08_N	I	GPIO_IN0	GPIO input 0
G14	GND	-	-	Signal Ground
G15	LA12_P	O	CH1_LED0	Link 1 Green indicator LED (Active low)
G16	LA12_N	O	CH1_LED1	Link 1 Red indicator LED (Active low)
G17	GND	-	-	Signal Ground
G18	LA16_P	I	CH1_PWRG	Channel 1 PoCXP power good indicator (Active high)
G19	LA16_N	I	CH0_PWRG	Channel 0 PoCXP power good indicator (Active high)
G20	GND	-	-	Signal Ground
G21	LA20_P	I	CH4_FLAGB	Channel 4 PoCXP indicator (Active high)
G22	LA20_N	I	CH3_FLAGB	Channel 3 PoCXP indicator (Active high)
G23	GND	-	-	Signal Ground
G24	LA22_P	O	CH3_ON	Channel 3 PoCXP enable (Active low)
G25	LA22_N	O	CH2_ON	Channel 2 PoCXP enable (Active low)
G26	GND	-	-	Signal Ground
G27	LA25_P	-	N/C	Not Connected
G28	LA25_N	-	N/C	Not Connected
G29	GND	-	-	Signal Ground
G30	LA29_P	-	N/C	Not Connected
G31	LA29_N	-	N/C	Not Connected
G32	GND	-	-	Signal Ground
G33	LA31_P	-	N/C	Not Connected
G34	LA31_N	-	N/C	Not Connected
G35	GND	-	-	Signal Ground

G36	LA33_P	-	N/C	Not Connected
G37	LA33_N	-	N/C	Not Connected
G38	GND	-	-	Signal Ground
G39	VADJ	-	VADJ	Adjustable voltage for I/O signals to FPGA
G40	GND	-	-	Signal Ground
H1	VREF_A_M2C	-	N/C	Not Connected
H2	PRSNT_M2C_L	-	GND	Pulled Low
H3	GND	-	-	Signal Ground
H4	CLK0_M2C_P	-	GND	Pulled to GND (Optionally connected to oscillator)
H5	CLK0_M2C_N	-	3.3V	Pulled to 3.3V (Optionally connected to oscillator)
H6	GND	-	-	Signal Ground
H7	LA02_P	I/O	LF4	CoaXPress channel 4 low speed link TX(2)/RX(1)
H8	LA02_N	I/O	LF3	CoaXPress channel 3 low speed link TX(2)/RX(1)
H9	GND	-	-	Signal Ground
H10	LA04_P	-	N/C	Not Connected
H11	LA04_N	O	AUTH_DIR_SDO 1	Direction selector for SDO1. High - output
H12	GND	-	-	Signal Ground
H13	LA07_P	O	GPIO_OUT5	GPIO output 5
H14	LA07_N	O	GPIO_OUT4	GPIO output 4
H15	GND	-	-	Signal Ground
H16	LA11_P	O	CH0_LED0	Link 0 Green indicator LED (Active low)
H17	LA11_N	O	CH0_LED1	Link 0 Red indicator LED (Active low)
H18	GND	-	-	Signal Ground
H19	LA15_P	O	CH4_LED0	Link 4 Green indicator LED (Active low)
H20	LA15_N	O	CH4_LED1	Link 4 Red indicator LED (Active low)
H21	GND	-	-	Signal Ground
H22	LA19_P	I	CH2_FLAGB	Channel 2 PoCXP indicator (Active high)
H23	LA19_N	I	CH1_FLAGB	Channel 1 PoCXP indicator (Active high)
H24	GND	-	-	Signal Ground
H25	LA21_P	O	CH1_ON	Channel 1 PoCXP enable (Active low)
H26	LA21_N	O	CH0_ON	Channel 0 PoCXP enable (Active low)
H27	GND	-	-	Signal Ground
H28	LA24_P	-	N/C	Not Connected
H29	LA24_N	-	N/C	Not Connected
H30	GND	-	-	Signal Ground
H31	LA28_P	-	N/C	Not Connected
H32	LA28_N	-	N/C	Not Connected
H33	GND	-	-	Signal Ground
H34	LA30_P	-	N/C	Not Connected
H35	LA30_N	-	N/C	Not Connected
H36	GND	-	-	Signal Ground
H37	LA32_P	-	N/C	Not Connected
H38	LA32_N	-	N/C	Not Connected
H39	GND	-	-	Signal Ground
H40	VADJ	-	VADJ	Adjustable voltage for I/O signals to FPGA
J1	GND	-	-	Signal Ground
J2	CLK1_C2M_P	-	N/C	Not Connected
J3	CLK1_C2M_N	-	N/C	Not Connected
J4	GND	-	-	Signal Ground
J5	GND	-	-	Signal Ground
J6	HA03_P	-	N/C	Not Connected
J7	HA03_N	-	N/C	Not Connected
J8	GND	-	-	Signal Ground
J9	HA07_P	-	N/C	Not Connected
J10	HA07_N	-	N/C	Not Connected
J11	GND	-	-	Signal Ground
J12	HA11_P	-	N/C	Not Connected

J13	HA11_N	-	N/C	Not Connected
J14	GND	-	-	Signal Ground
J15	HA14_P	-	N/C	Not Connected
J16	HA14_N	-	N/C	Not Connected
J17	GND	-	-	Signal Ground
J18	HA18_P	-	N/C	Not Connected
J19	HA18_N	-	N/C	Not Connected
J20	GND	-	-	Signal Ground
J21	HA22_P	-	N/C	Not Connected
J22	HA22_N	-	N/C	Not Connected
J23	GND	-	-	Signal Ground
J24	HB01_P	-	N/C	Not Connected
J25	HB01_N	-	N/C	Not Connected
J26	GND	-	-	Signal Ground
J27	HB07_P	-	N/C	Not Connected
J28	HB07_N	-	N/C	Not Connected
J29	GND	-	-	Signal Ground
J30	HB11_P	-	N/C	Not Connected
J31	HB11_N	-	N/C	Not Connected
J32	GND	-	-	Signal Ground
J33	HB15_P	-	N/C	Not Connected
J34	HB15_N	-	N/C	Not Connected
J35	GND	-	-	Signal Ground
J36	HB18_P	-	N/C	Not Connected
J37	HB18_N	-	N/C	Not Connected
J38	GND	-	-	Signal Ground
J39	VIO_B_M2C	-	3.3V	Connected to 3.3V
J40	GND	-	-	Signal Ground
K1	VREF_B_M2C	-	N/C	Not Connected
K2	GND	-	-	Signal Ground
K3	GND	-	-	Signal Ground
K4	CLK1_M2C_P	-	GND	Pulled to GND
K5	CLK1_M2C_N	-	VADJ	Adjustable voltage for I/O signals to FPGA
K6	GND	-	-	Signal Ground
K7	HA02_P	-	N/C	Not Connected
K8	HA02_N	-	N/C	Not Connected
K9	GND	-	-	Signal Ground
K10	HA06_P	-	N/C	Not Connected
K11	HA06_N	-	N/C	Not Connected
K12	GND	-	-	Signal Ground
K13	HA10_P	-	N/C	Not Connected
K14	HA10_N	-	N/C	Not Connected
K15	GND	-	-	Signal Ground
K16	HA17_P_CC	-	N/C	Not Connected
K17	HA17_N_CC	-	N/C	Not Connected
K18	GND	-	-	Signal Ground
K19	HA21_P	-	N/C	Not Connected
K20	HA21_N	-	N/C	Not Connected
K21	GND	-	-	Signal Ground
K22	HA23_P	-	N/C	Not Connected
K23	HA23_N	-	N/C	Not Connected
K24	GND	-	-	Signal Ground
K25	HB00_P_CC	-	N/C	Not Connected
K26	HB00_N_CC	-	N/C	Not Connected
K27	GND	-	-	Signal Ground
K28	HB06_P_CC	-	N/C	Not Connected
K29	HB06_N_CC	-	N/C	Not Connected
K30	GND	-	-	Signal Ground

K31	HB10_P	-	N/C	Not Connected
K32	HB10_N	-	N/C	Not Connected
K33	GND	-	-	Signal Ground
K34	HB14_P	-	N/C	Not Connected
K35	HB14_N	-	N/C	Not Connected
K36	GND	-	-	Signal Ground
K37	HB17_P_CC	-	N/C	Not Connected
K38	HB17_N_CC	-	N/C	Not Connected
K39	GND	-	-	Signal Ground
K40	VIO_B_M2C	-	3.3V	Connected to 3.3V

Table 2 : FMC connector pin assignments

(1) Used when channel is assembled as transmitter (Device)
(2) Used when channel is assembled as receiver (Host)

5.2 FMC connector standard pin assignments

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK1_C2M_P	PRSNT_M2C_L	CLK0_C2M_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK1_C2M_N	GND	CLK0_C2M_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK1_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK1_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table 3 : FMC connector standard pin assignments

5.3 DIN Connector pin assignment

Connector	Channel
J5	0
J6	1
J7	2
J8	3
J9	4

Table 4 : DIN connector pin assignment

5.4 External power connector pin assignments (J26)

Pin	Signal
1	12V
2	12V
3	12V
4	12V
5	GND
6	GND
7	GND
8	GND

Table 5 : External power connector pin assignment (J26)

- Used connector is GPIO PN- 053398-0871 from Molex

5.5 Schematic of channel when used as receiver (Host)

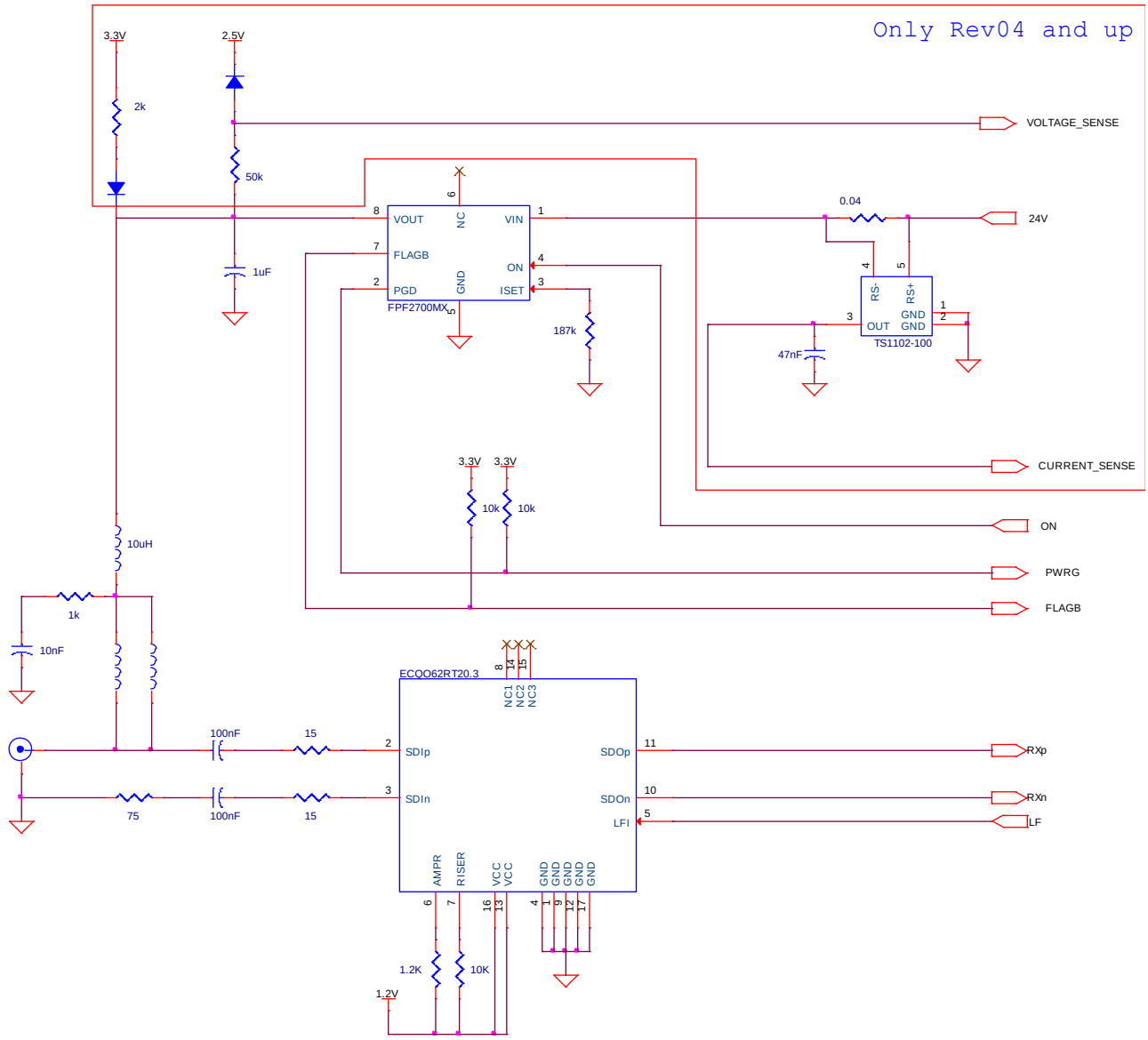

Figure 4 : Schematic of channel when used as receiver

CHx_PWRG – active high, indicates that the output voltage from the power source (FPF2700MX) reached 90% of the input voltage.

CHx_FLAGB – active low, indicates that either the current limit was reached or that there is an under-voltage issue or that the power source (FPF2700MX) over heated.

5.6 Schematic of channel when used as transmitter (Device)

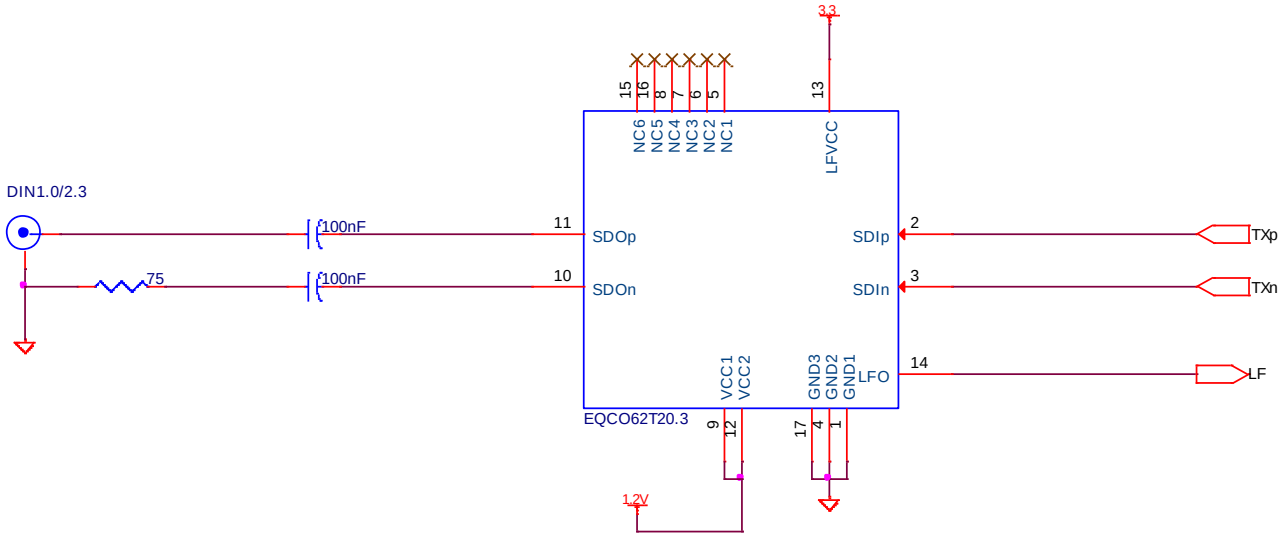

Figure 5 : Schematic of channel when used as transmitter

5.7 GPIO Connector pin assignments (J21)

Pin	Signal
1	GPIO OUT 0
2	GPIO OUT 1
3	GPIO OUT 2
4	GPIO OUT 3
5	GPIO OUT 4
6	GPIO OUT 5
7	GPIO GND
8	GPIO GND
9	GPIO IN 0
10	GPIO IN 1
11	GPIO IN 2
12	GPIO IN 3
13	GPIO IN 4
14	GPIO IN 5

Table 6 : GPIO Connector pin assignments (J21)

- Used connector is GPIO PN-053398-1471 from Molex

5.8 GPIO isolation schematics (optional, up to rev 4 only)

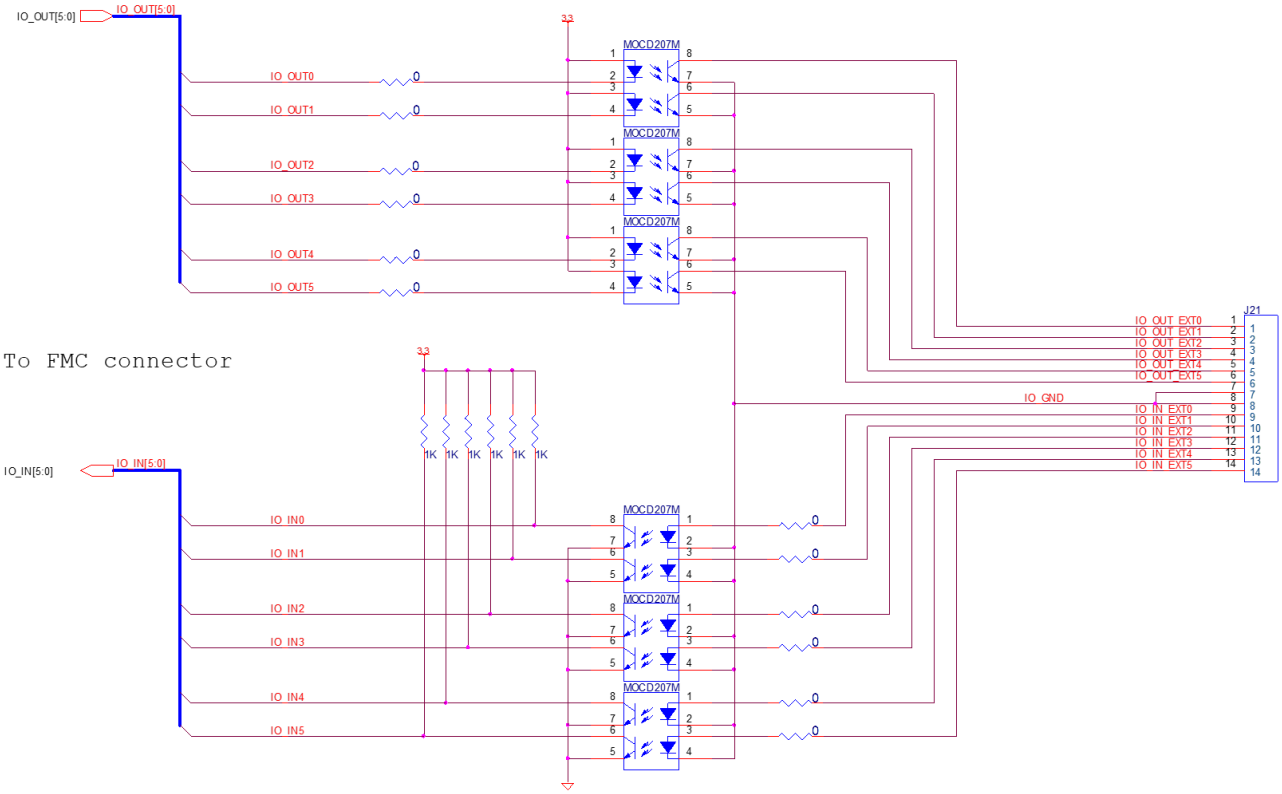

Figure 6 : GPIO isolation schematics

5.9 CoaXPress cables

CoaXPress is a new digital transmission standard that allows high speed data from a device, such as a camera, to be transferred to a host, such as a frame grabber. Each CoaXPress link supports up to 6.25 Gbps data rates, along with device power up to 13W and device control at 20 Mbps – all on a single coax cable. For very fast devices, the links can be aggregated to provide multiples of the single coax bandwidth. Long cable lengths are supported – up to 40 meters at 6.25 Gbps and over 100 meters at 3.125 Gbps.

Table 7 gives an overview of typical link performance at room temperature for the link between two KY-FMCCXP boards, using the downlink channel, uplink channel and power transmission simultaneously.

BELDEN

	Name	Belden 7731A	Belden 1694A	Belden 1505A	Belden 1505F	Belden 1855A
	Type	Long Distance	Industry Standard	Compromis Coax	Flexible	Thinnest cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
1.25 Gbps	(m)	194	130	107	80	55
2.5 Gbps	(m)	162	110	94	66	55
3.125 Gbps	(m)	147	100	86	60	55
5.0 Gbps	(m)	87	60	52	35	38
6.25 Gbps	(m)	58	40	35	23	25

GEPCO

	Name	Gepco VHD1100	Gepco VSD2001	Gepco VPM2000	Gepco VHD2000M	Gepco VDM230
	Type	Long Distance	Industry Standard	Compromis Coax	Flexible	Thinnest cable
Diameter	(mm)	10.3	6.91	6.15	6.15	4.16
1.25 Gbps	(m)	212	140	109	81	66
2.5 Gbps	(m)	185	120	94	67	66
3.125 Gbps	(m)	169	110	86	61	62
5.0 Gbps	(m)	102	66	53	36	38
6.25 Gbps	(m)	68	44	35	24	25

Table 7 : Typical link performance

6.1 Absolute maximum ratings

Specification	Values
3.3V power supply	-0.5V to 3.6V
VADJ power supply	-0.5V to 3.6V
12V power supply	-0.5V to 14V
Storage Temperature	-55 °C to 150 °C
Operating Temperature	-40°C to 85 °C
Voltage on high speed serial lines	-0.5V to 1.6V
Voltage on LF signals	-0.5V to 3.6V
Leds voltage	-0.5V to 3.6V
GPIO Voltage (FPGA Side)	(1)
GPIO Voltage (External Side)	-0.5V to 26V (2)

Table 8 : Absolute maximum ratings

(1) The GPIO voltage is set according to the FPGA specifications.

(2) The maximum value of 26V is possible only when the optional opto-isolated transistors are used. By default, those transistors are bypassed by 0ohm (1/16W) resistors, please see remark (1) for the maximum voltages in this case.

6.2 Operating conditions

Parameter	Description	Minimum	Typical	Maximum
3.3V VCC	Supply voltage	3.14V	3.3V	3.46V
VADJ [1]	Supply voltage	1.1		3.46
12V VCC	Supply voltage	11.4V	12V	12.6V
Is 3.3V	Supply Current		15mA	100mA
Is 12V	Supply Current		21mA	[2]
Ishort	Short circuit trigger current		0.9A	
LF VIL	Input LOW Voltage		0V	
LF VIH	Input HIGH Voltage		VADJ	
LF VOL	Low output level		0V	
LF VOH	High output level		VADJ	
DVo	Output differential amplitude on RX		1200mV	
DVi	Input differential amplitude on TX	500mV	600mV	
GPIO FVIL	Low level input voltage on GPIO (FPGA)	-0.5V	0V	[3]
GPIO FVIH	High level input voltage on GPIO (FPGA)	[3]		
GPIO VIL	Low level input voltage on GPIO	-0.5V	0V	[3]
GPIO VIH	High level input voltage on GPIO	[3]		
GPIO FVOL	Low level output voltage on GPIO (FPGA)		0V	
GPIO FVOH	High level output voltage on GPIO (FPGA)	[3]		
LED Von	Led ON voltage	[3]		

Table 9 : Operating conditions

[1] Revision 4 and older CXP mezzanine cards can support only Vadj voltage of 2.5V and higher. Rev 5 and newer cards, can support the entire range of voltages (1.2V – 3.3V).

[2] The maximum power consumption on 12V depends on power output on the receiver channels.

[3] The GPIO voltage is set according to the FPGA specifications.

7.1 Available Configurations

The ***FPGA Mezzanine Card for CoaXPress™*** board is available in various configurations depending on the number of cameras you want to connect as a Host or Device Links.

Model	Host Links	Device Links
KY-FMCCXP-2R3T	2	3
KY-FMCCXP-4R1T	4	1
KY-FMCCXP-4T1R	1	4

Table 10 : Available Configurations

The order of the channels is according to the model name, i.e. “KY-FMCCXP-2R3T” has 2 host links (Rx) and 3 device links (Tx), channel 0 and channel 1 are the host links and channels 2, 3 and 4 are device links.

7.2 Installation instructions

1. Before installing, turn of the power to the board.
2. Firmly press the FPC connector to the FMC carrier board.
3. Use spacers if the FMC is not aligned correctly with the carrier board.
4. Configure the FPGA board VADJ to match the selected FPGA I/O standard