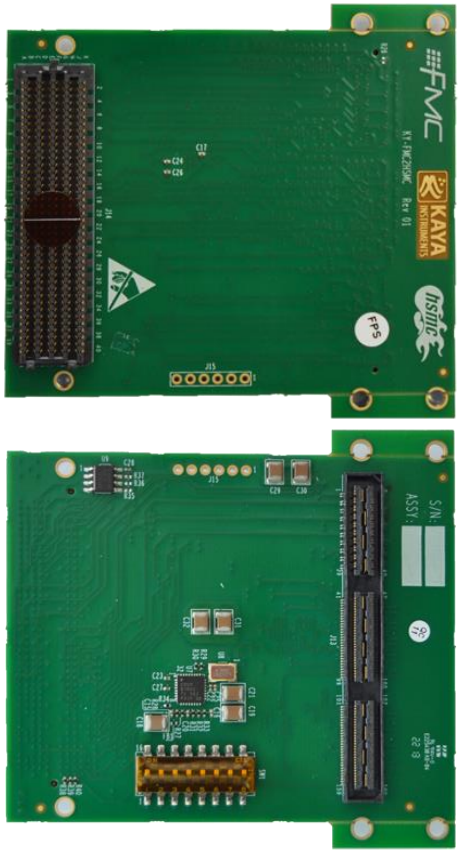
FPGA Mezzanine Card (FMC) to High Speed Mezzanine Card (HSMC) adapter board (KY-FMC2HSMC)

Overview

The FMC2HSMC is an adapter board designed to enable connection of industry standard HSMC cards to FPGA boards with FMC interface. This adapter board is designed to support full duplex high speed serial signals (SerDes), as well as LVDS or single ended signals. The FMC2HSMC uses a standard HPC connector as an interface to the host board and a standard HSMC connector as an interface to the mezzanine card.



About FMC

FPGA mezzanine card, or FMC, as defined in VITA 57.1, provides a specification describing an I/O mezzanine module with connection to an FPGA or other device with reconfigurable I/O capability. The FMC standard describes a versatile module, which can target a range of applications, environments, and markets. The specification defines a commercial grade version, which extends to cover a ruggedized conduction variant. FPGA's provide a high pin count that can operate at many Gbps. The latest connector technology is defined to maintain the high performance interface from the I/O on the mezzanine module, to the FPGA on the carrier card. The FMC mezzanine module design minimizes design effort and resources through minimal system support and flexible pin allocation.

About HSMC

The Altera high speed mezzanine card (HSMC) specification defines the electrical and mechanical properties of a high speed mezzanine card adapter interface for FPGA-based motherboards. This specification should allow for the design of interoperable motherboards and add-on cards by different manufacturers that can interoperate and utilize the high-performance I/O features found in today's FPGA devices.

Features

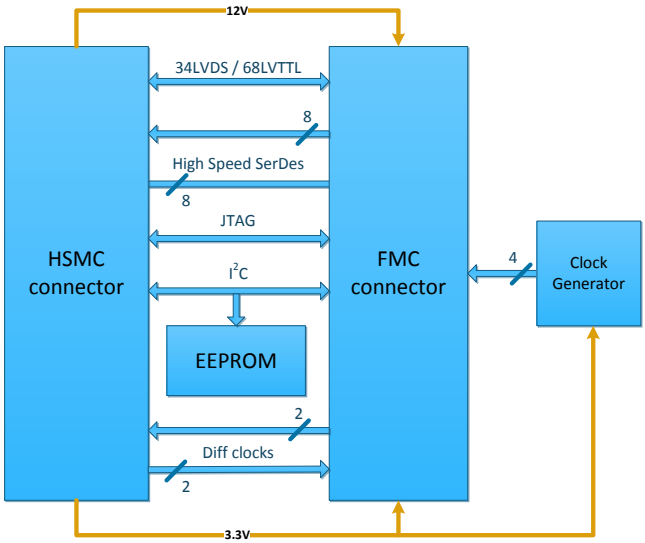
- Enables connection of standard HSMC cards to FMC enabled FPGA boards
- Interfaces:
  - Up to 8 full duplex high speed serial channels with HPC
  - Up to 1 full duplex high speed serial channels with LPC
  - Up to 34 LVDS channels or 68 single ended LVTTL signals connected to FMC connector
- Altera HSMC compliant
- FMC (VITA 57.1) compliant
- Support HPC or LPC FMC
- Supports air and conduction cooling FMC
- -40°C to 85°C operating environment temperature (industrial grade)

Clocks

On Board, user programmable, low jitter clock generator used to provide clock reference as required for high speed links. The clock frequency can be selected from the following:

- 100 MHz, supporting PCIe gen 1
- 125 MHz, supporting PCIe gen 1, GigE, Aurora and SRIO 1.25 and 2.5 Gbps
- 150 MHz, supporting SATA
- 156.25 MHz, supporting XAUI, SRIO and Aurora 3.125 Gbps
- 250 MHz, supporting PCIe gen 2
- 312.5 MHz, supporting Aurora 5 and 6.25 Gbps

Block Diagram



Applications

- ✓ Analog to digital conversion
- ✓ Digital to analog conversion
- ✓ Interface peripherals (HD/SD/SDI/SFP/PCIe/SMA etc.)
- ✓ Serial connectivity (LVDS/Serdes etc.)
- ✓ Image processing (HDMI/ DVI/ DP/ LVDS etc.)
- ✓ Machine vision (CameraLink/CXP etc.)
- ✓ Industrial interfaces

Deliverables

- FMC to HSMC adapter board (KY-FMC2HSMC)
- Hardware user manual

Accessories

- KY-CBLHSMC3 – 3.75” extension cable
- KY-CBLHSMC6 – 6” extension cable

Contact

sky blue microsystems

Sky Blue Microsystems GmbH
Geisenhausenerstr. 18
81379 Munich, Germany
+49 89 780 2970, info@skyblue.de
www.skyblue.de

ZERIF TECHNOLOGIES LTD.
A SKY BLUE COMPANY, FOUNDED 1999

In Great Britain:
Zerif Technologies Ltd.
H5 Ash Tree Court
Nottingham NG8 6PY, England
+44 115 855 7883, info@zerif.co.uk
www.zerif.co.uk