FPGA Authentication IP core

Overview

KAYA Instruments' FPGA authentication IP Core is a cost effective way to protect FPGA designs and FPGA IPs against piracy cloning and tampering. The IP Core uses an external BQ26100 authentication chip from TI and communicates with it using one wire interface. The IP Core uses an SHA-1 challenge and response authentication scheme that is judged to be one of the most secure schemes available. A random message is used each time to avoid tampering of the one wire interface; the randomization of the message can be synchronized to a random data source such as PLL or user traffic. All the leading industry FPGA and CPLD vendors are supported.

Features

- Protection for FPGA code and IP
- Reverse engineering proof
- SHA-1 secure authentication scheme
- Random challenge for increased protection
- Support for BQ26100 authentication chip
- One wire communication for reduced I/O usage
- Support for Altera®, Xilinx® and Lattice® FPGAs and CPLDs
- Operating frequency of up to 160Mhz
- Small logic footprint
- Compatible with BQ26100EVM development board for evaluation

Applications

- ✓ FPGA based devices
- ✓ Intellectual property

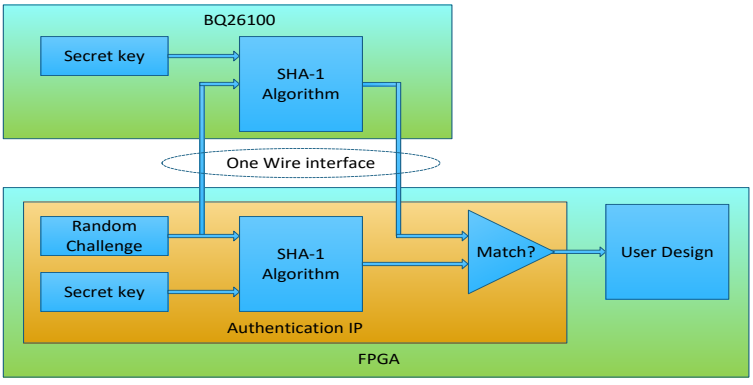
Core Details

- Single or multi-use license
- Soft IP core: RTL-encrypted source code, synthesis scripts, etc.
- Language: Verilog and VHDL
- Support for Altera®, Xilinx® and Lattice® FPGAs and CPLDs

Deliverables

- FPGA Authentication IP Core
- User Manual

Block Diagram



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